

FIG. 1
PRIOR ART

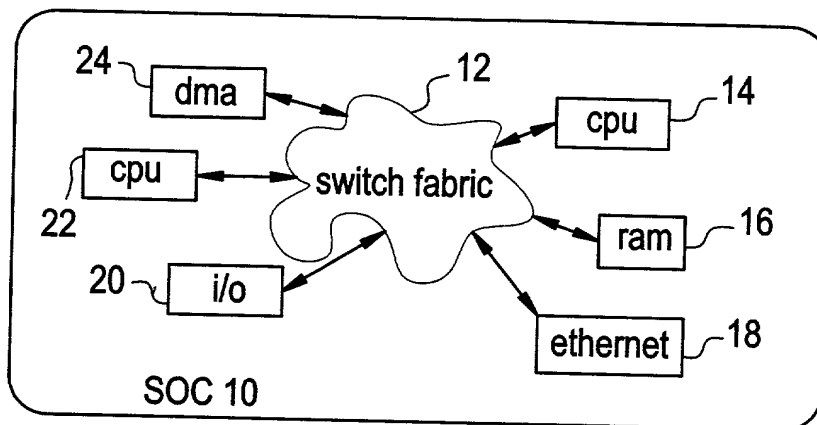


FIG. 2

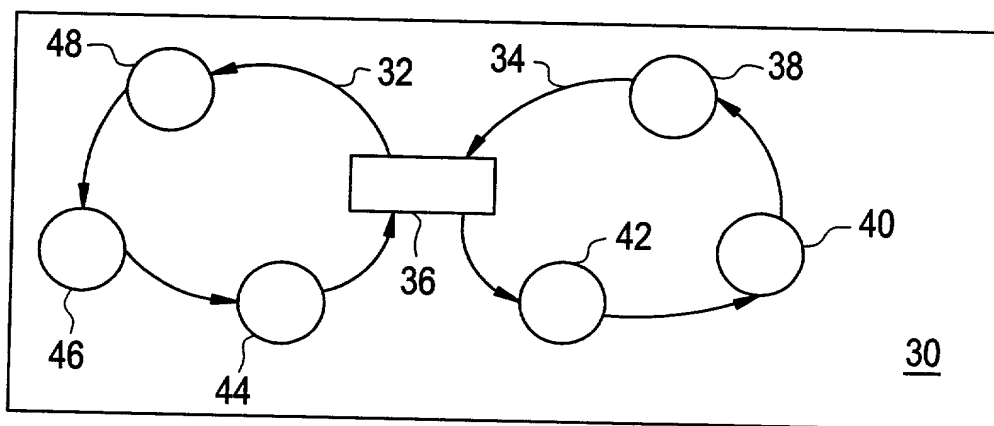


FIG. 3

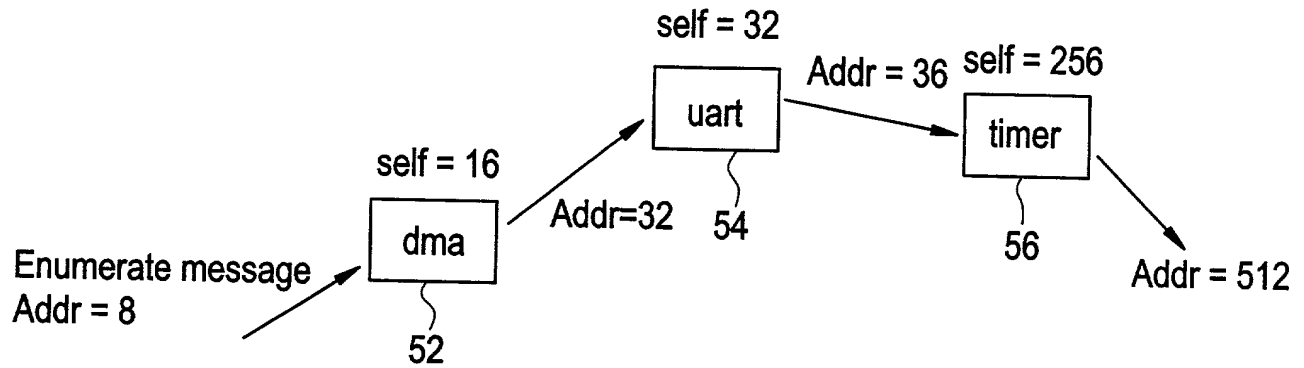


FIG. 4

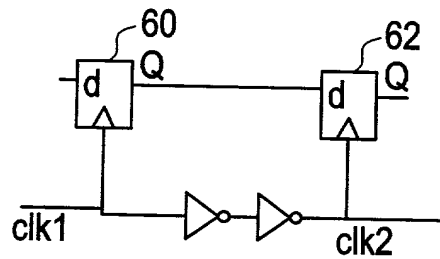


FIG. 5

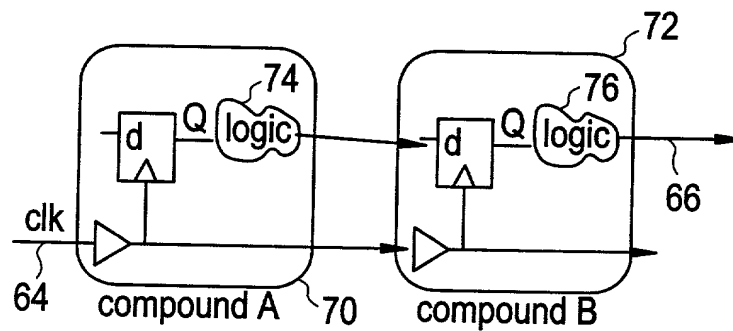


FIG. 6

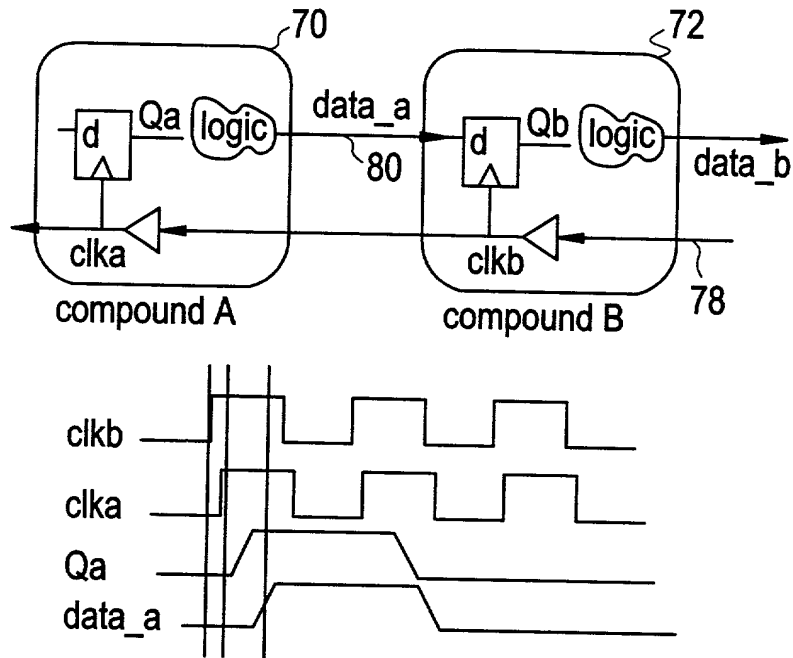


FIG. 7

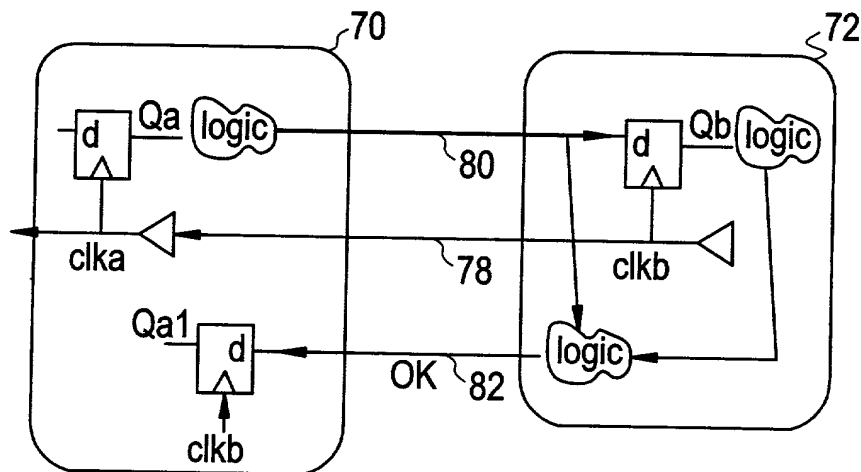


FIG. 8

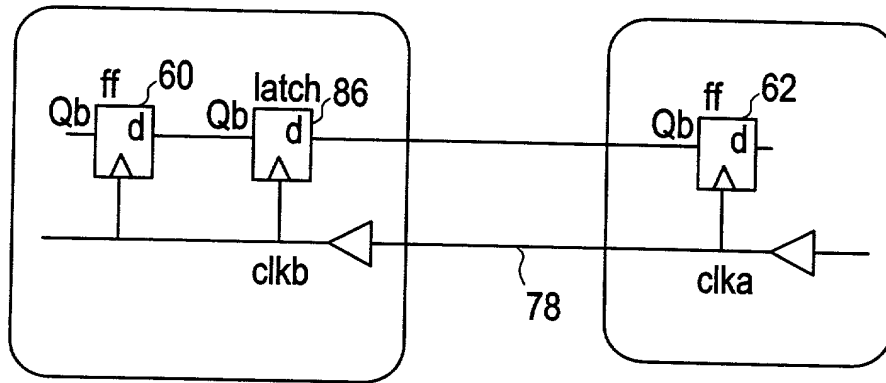


FIG. 9

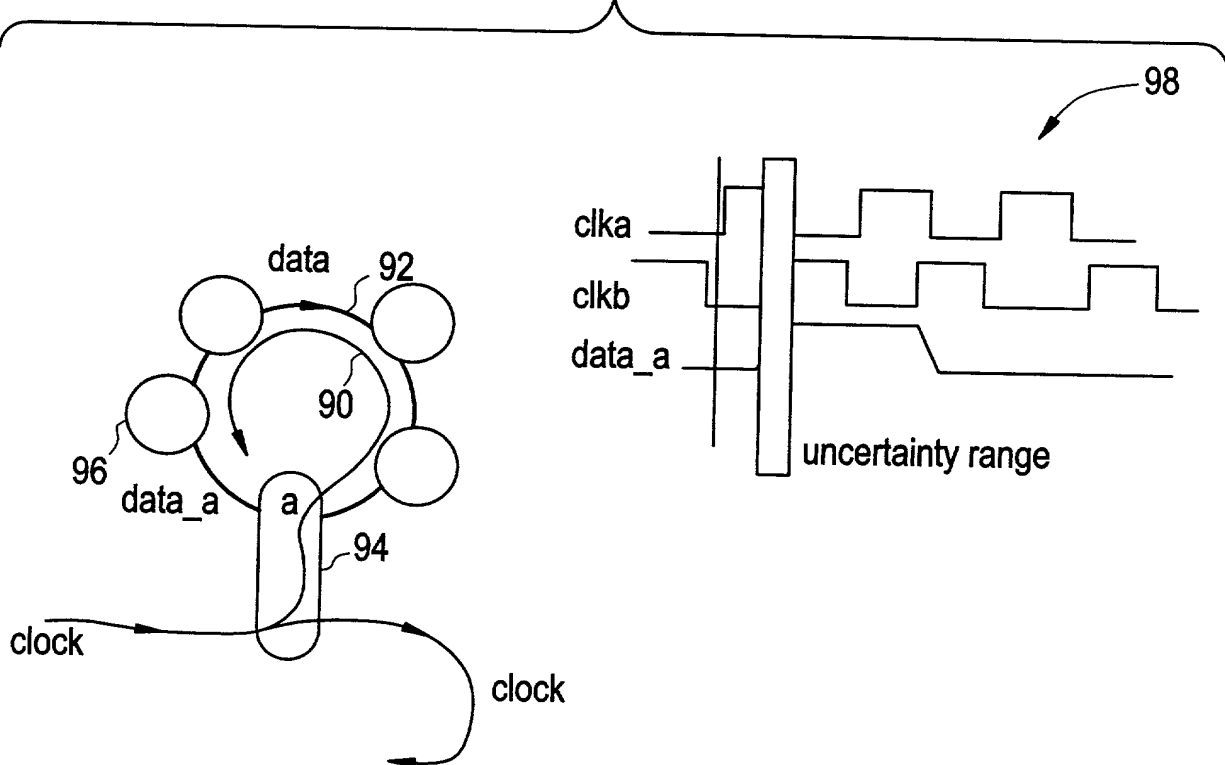


FIG. 10

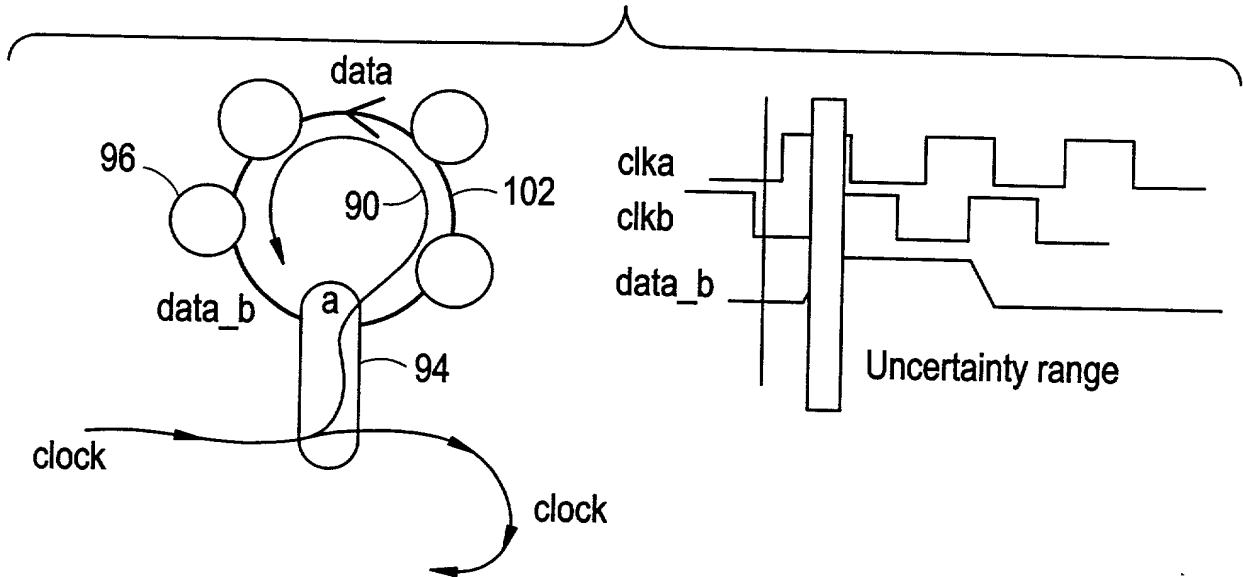


FIG. 11

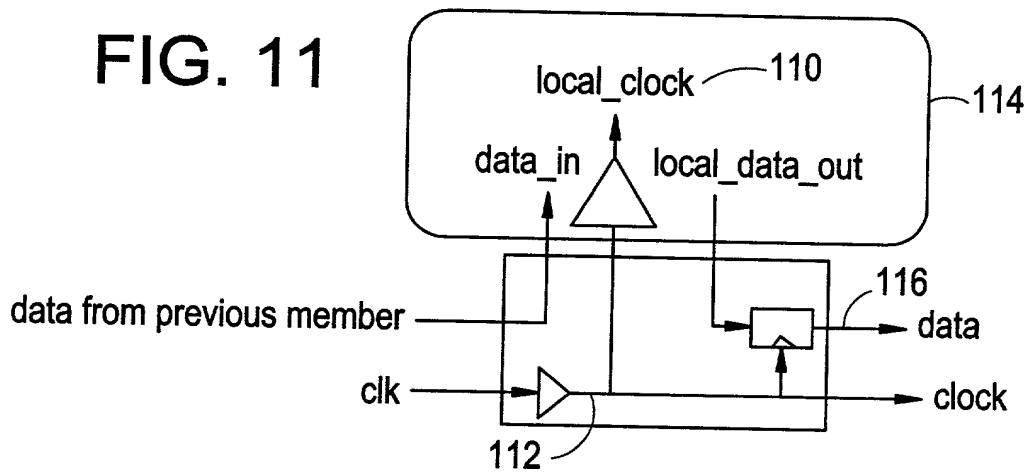


FIG. 12

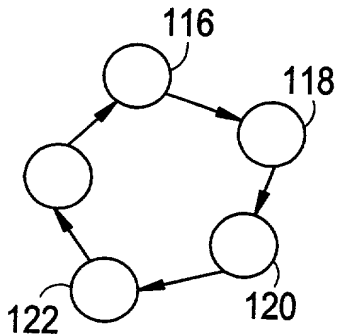


FIG. 13

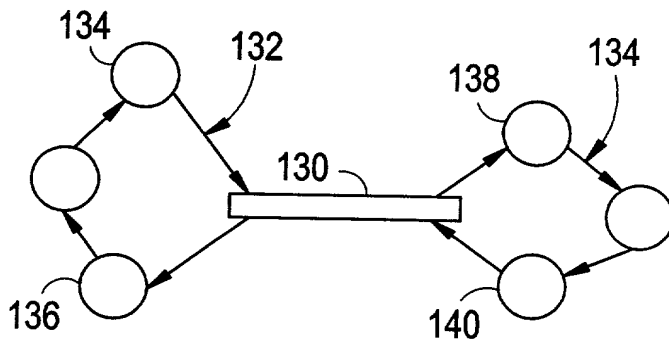


FIG. 14

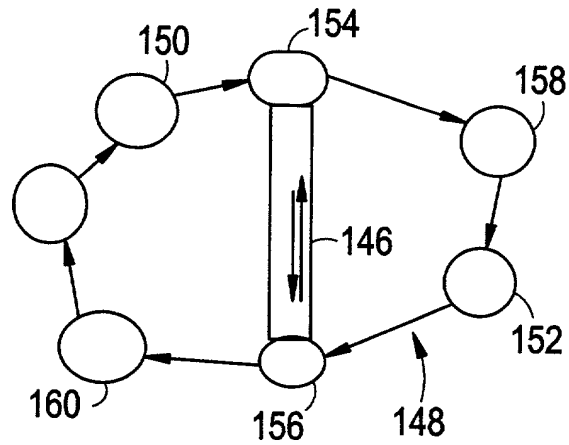


FIG. 15

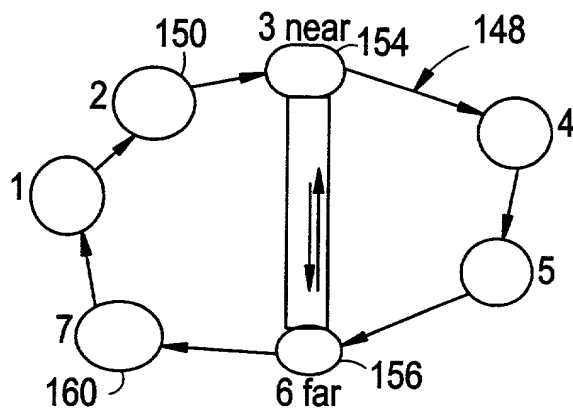


FIG. 16

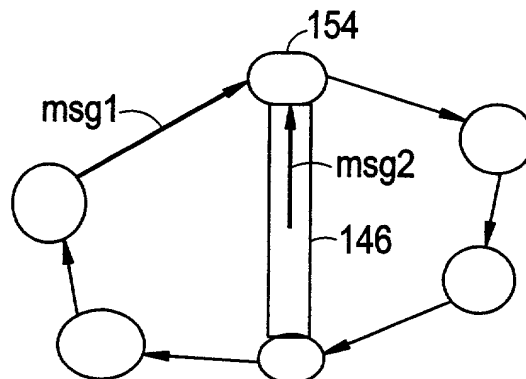


FIG. 17

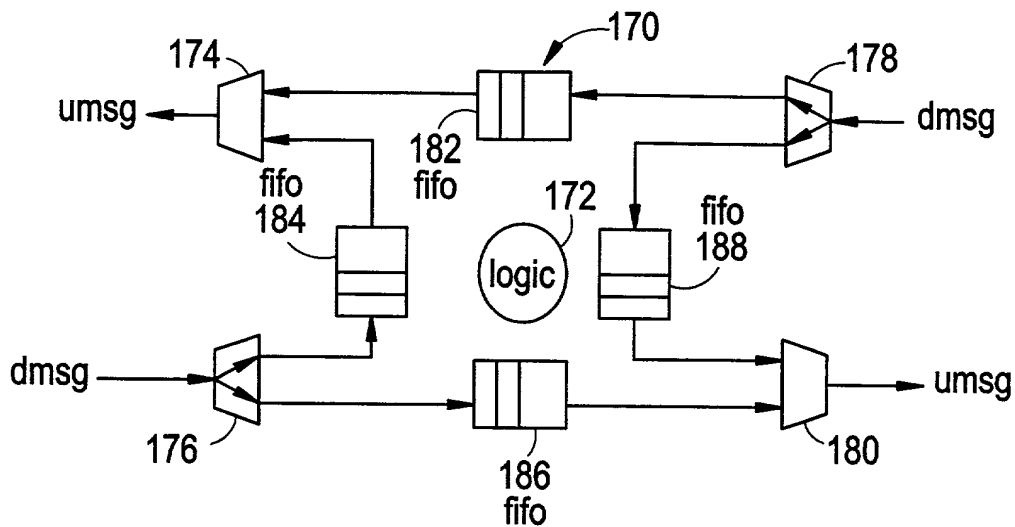


FIG. 18

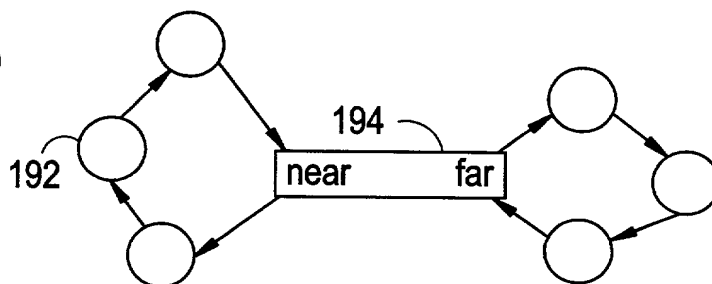


FIG. 19

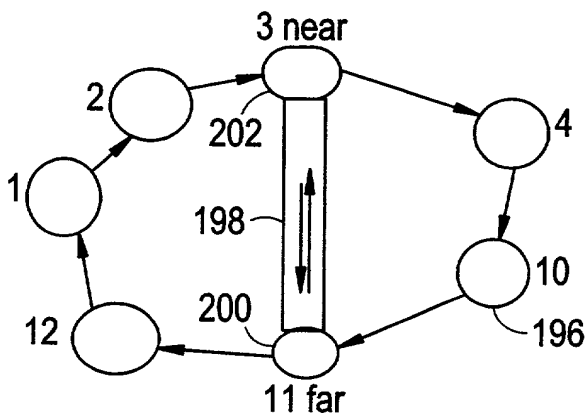


FIG. 20

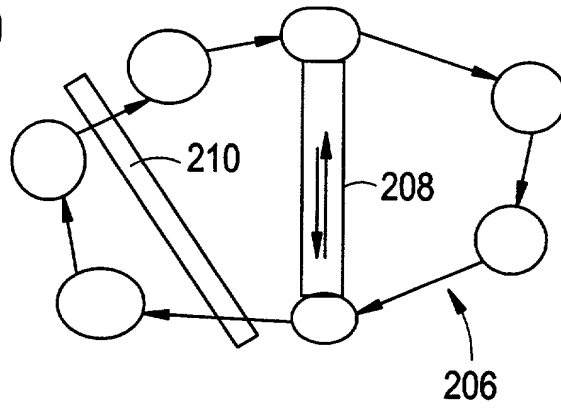


FIG. 21

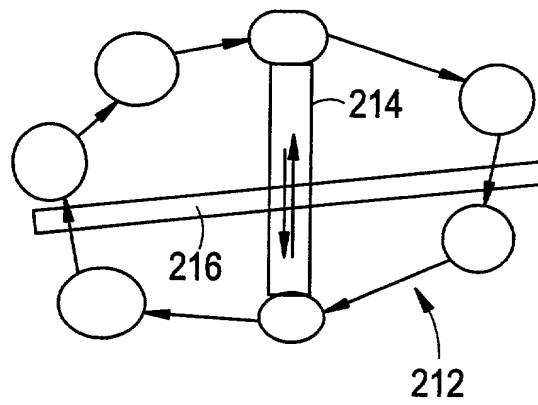
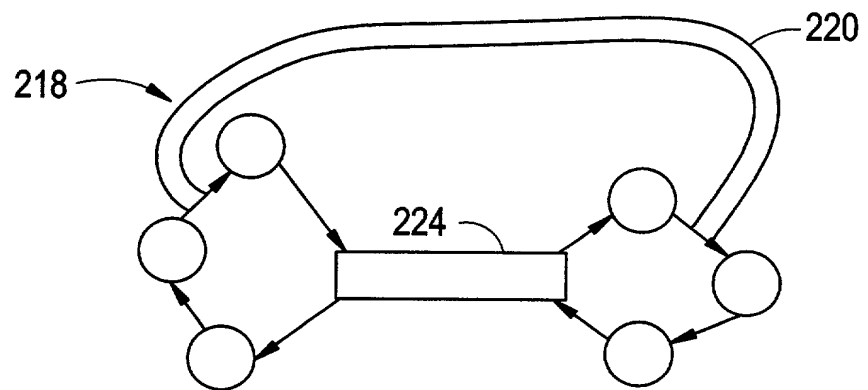


FIG. 22



9/64

FIG. 23

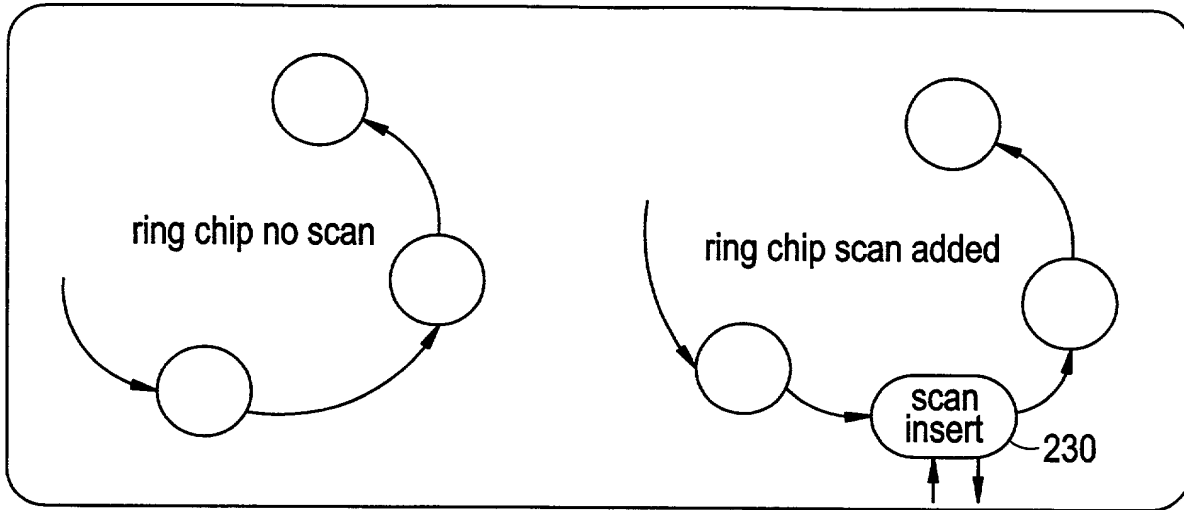


FIG. 24

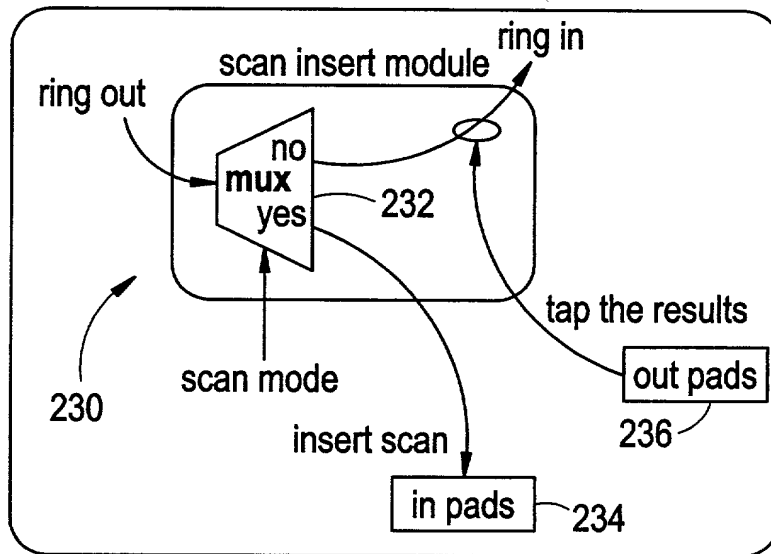


FIG. 25

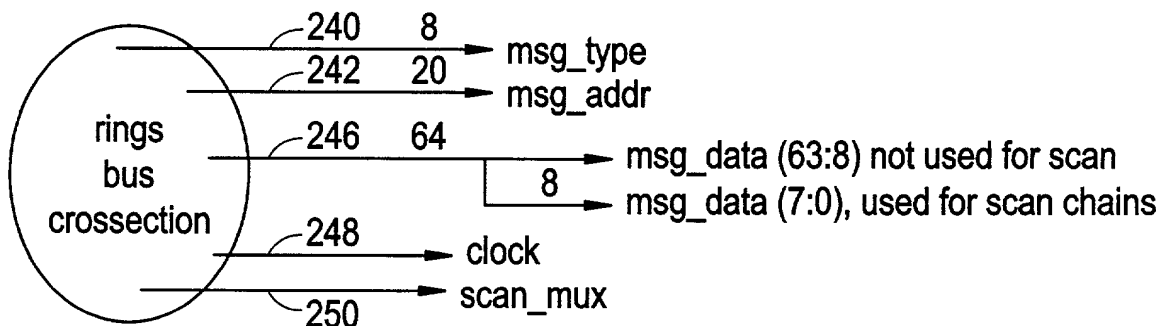


FIG. 26

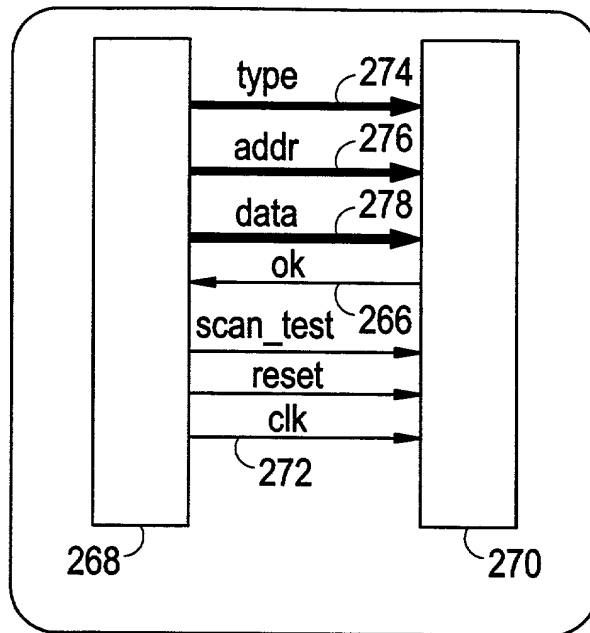


FIG. 27

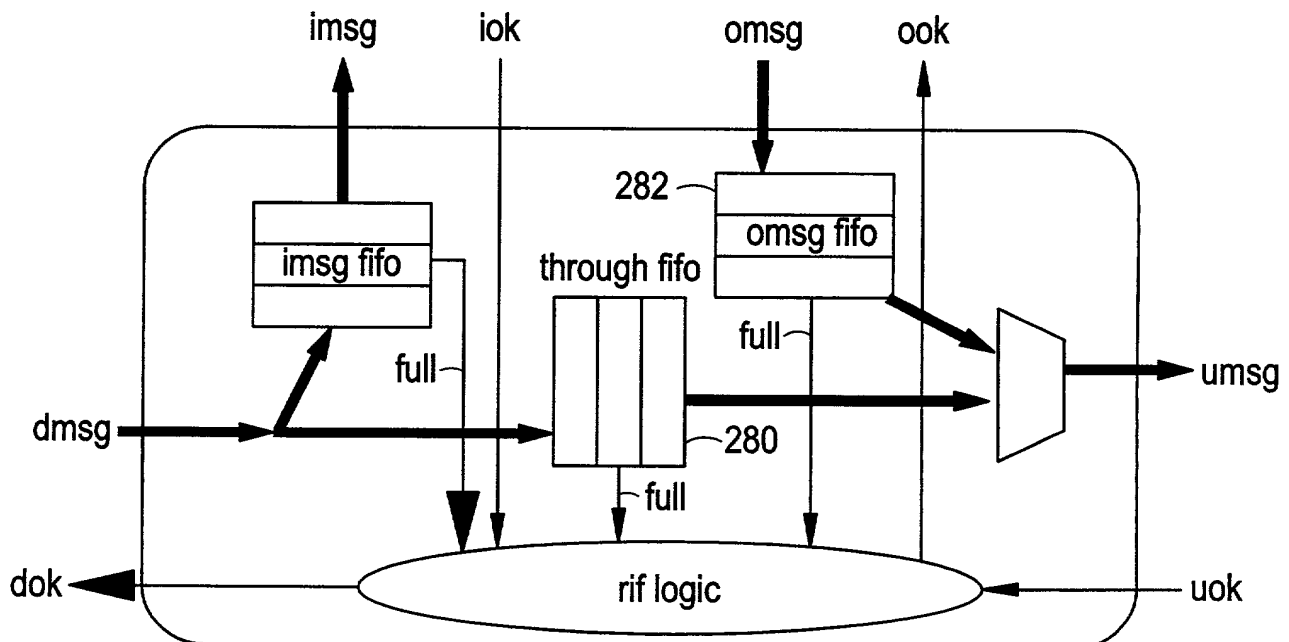


FIG. 28

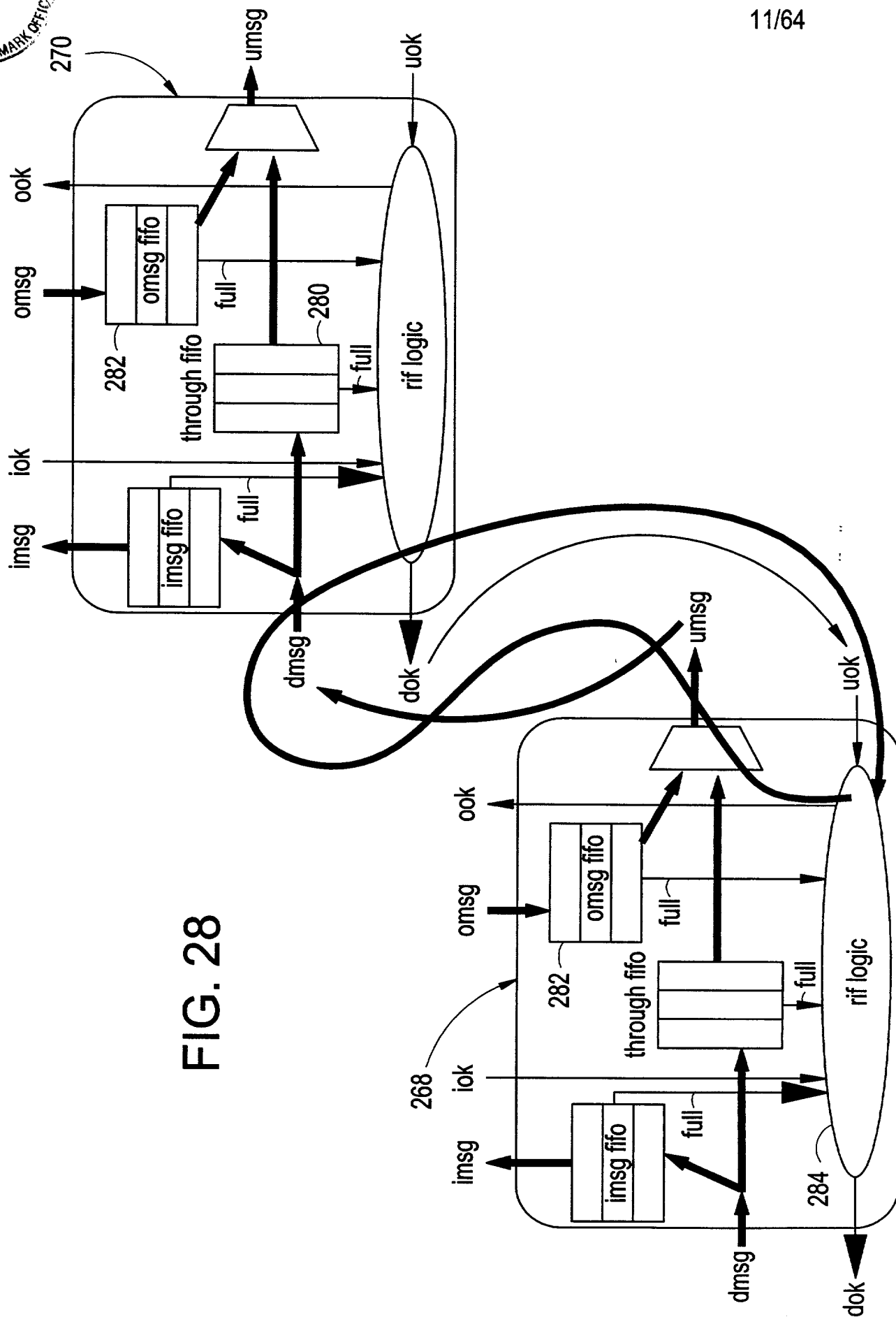


FIG. 29

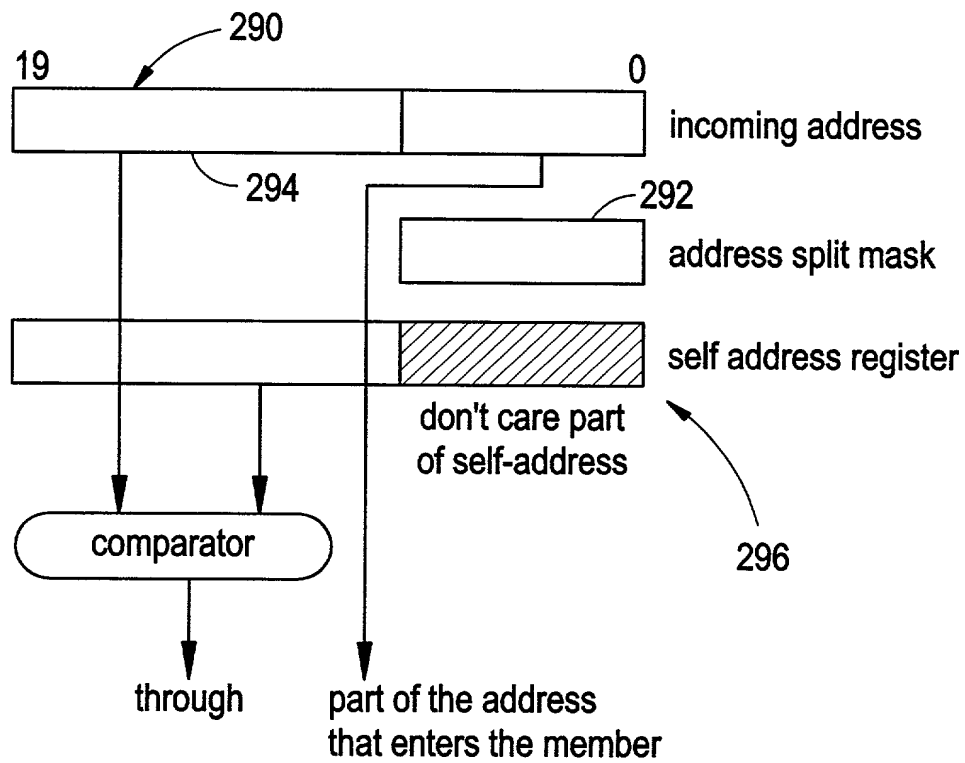


FIG. 30

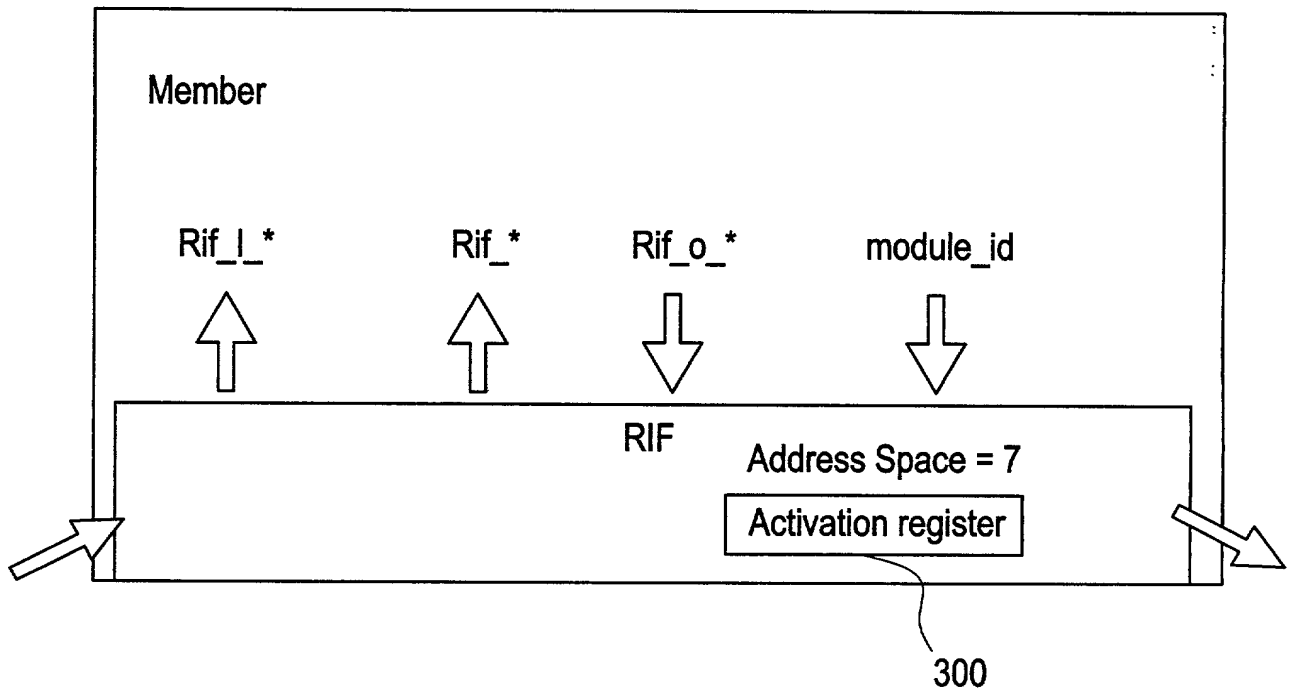


FIG. 31

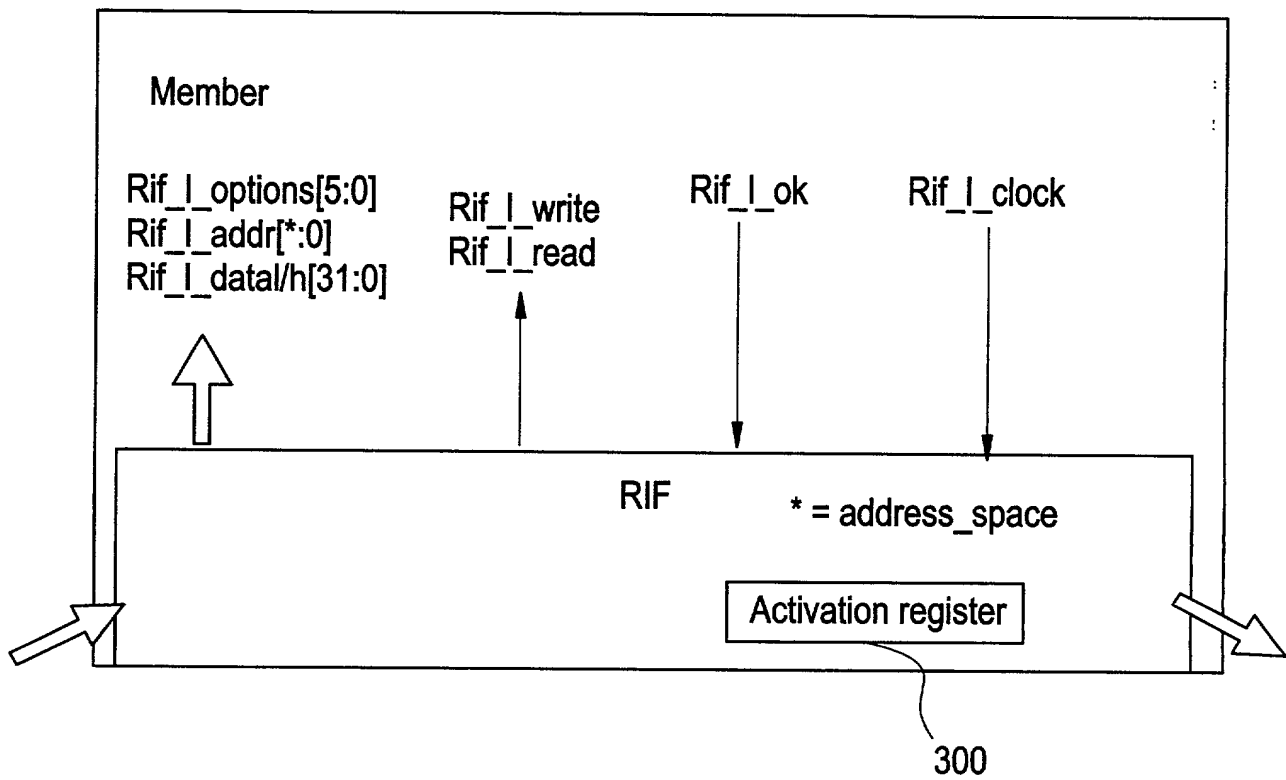


FIG. 32

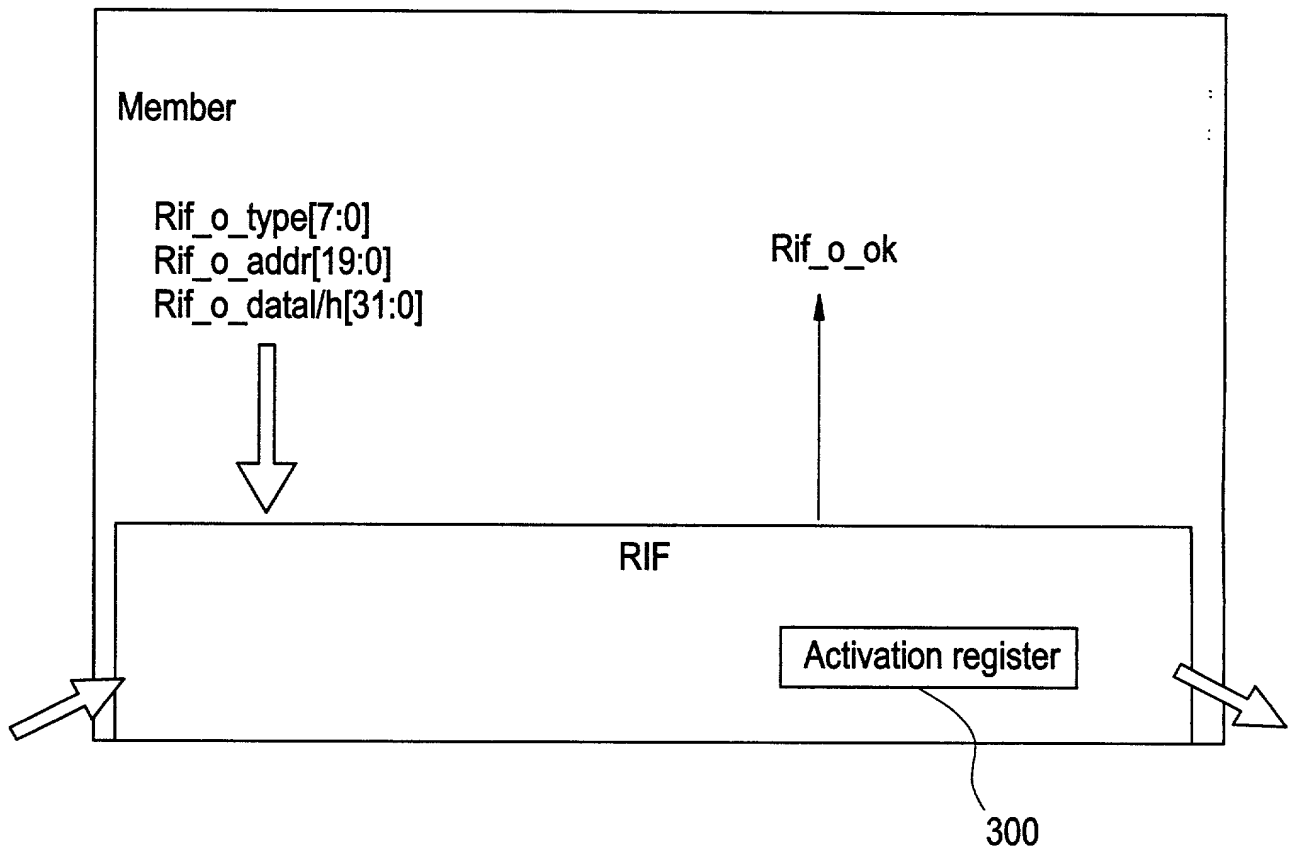


FIG. 33

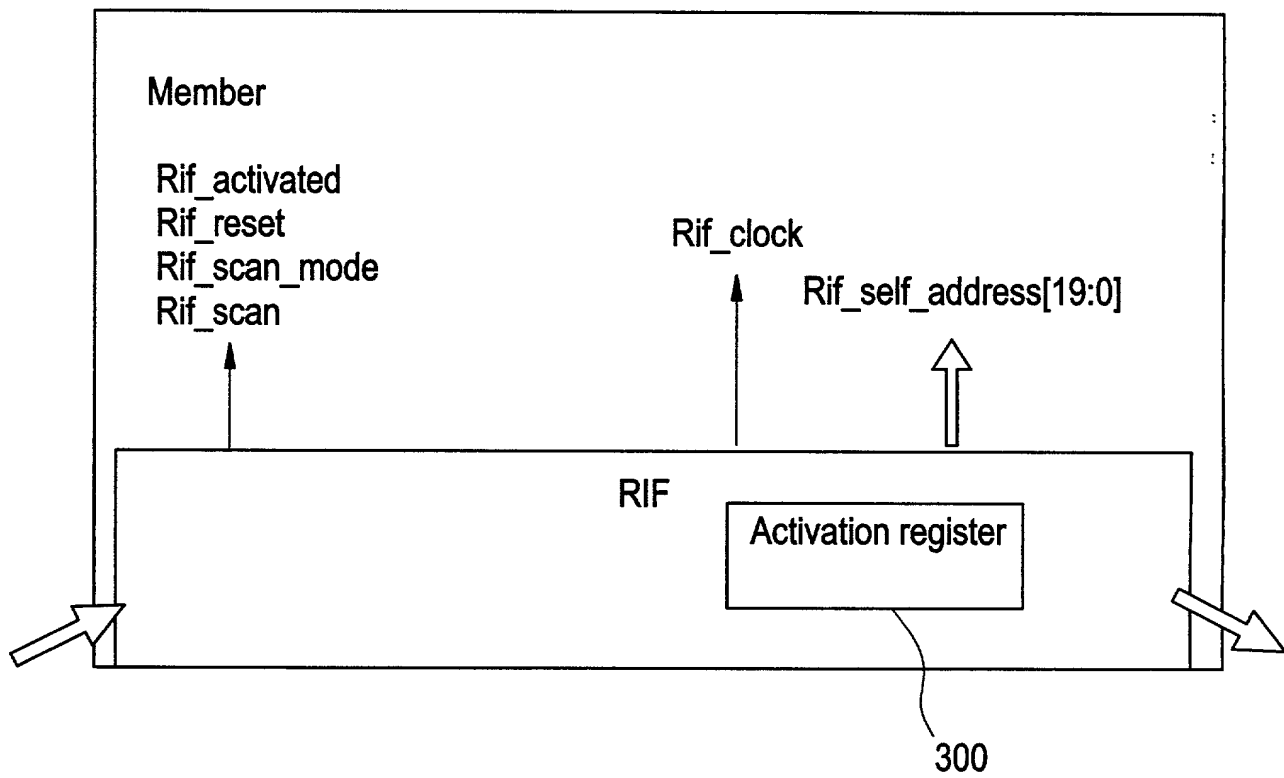
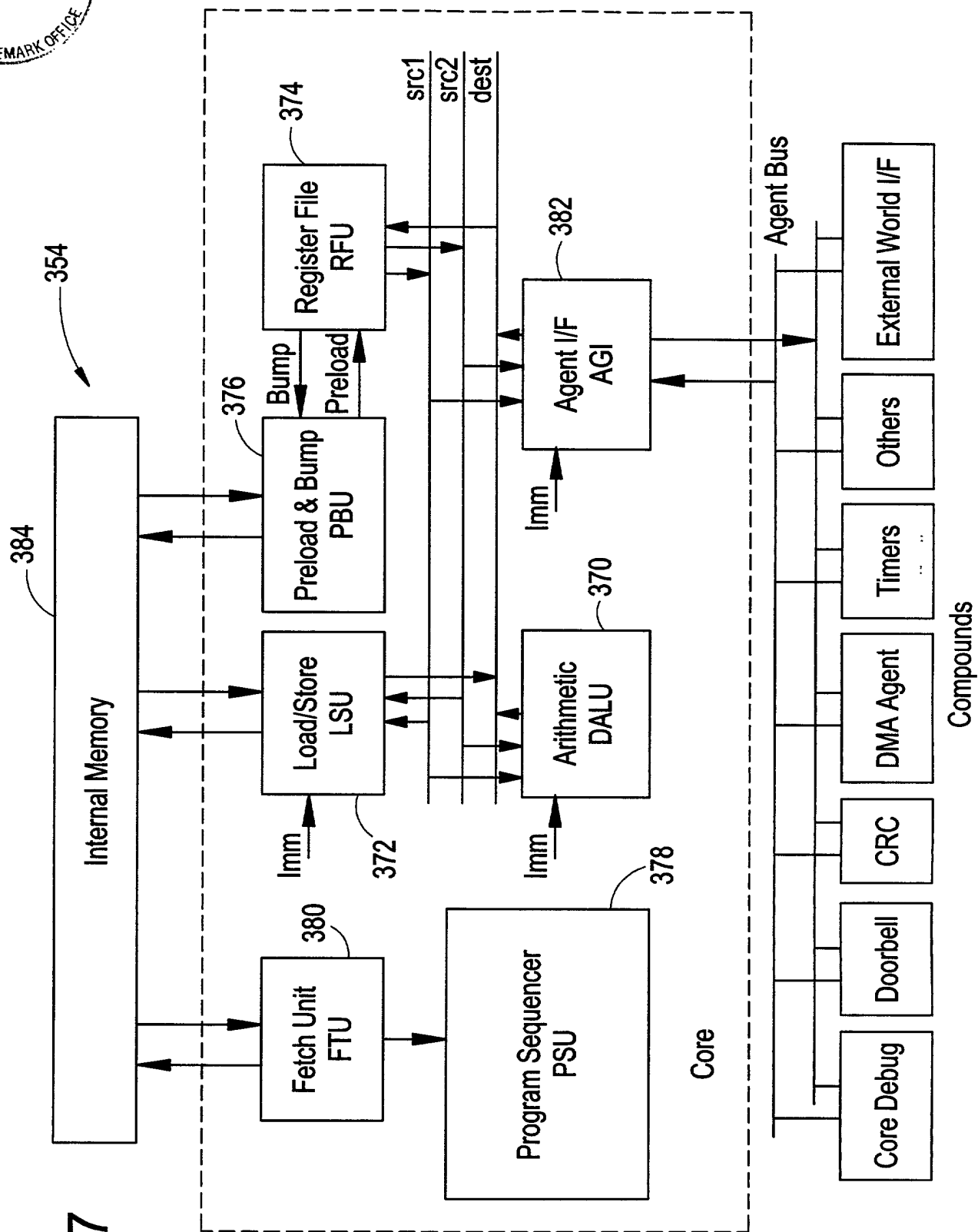


Figure 1: Block diagram of the system architecture. A 'chip' block contains a 'vobla' block and a 'bridge' block. The 'vobla' block is connected to the 'bridge' block via a circular path. The 'bridge' block is connected to a '340' block via a circular path. The '340' block is connected to an 'FPGA' block via two lines labeled 'utopia tx' and 'utopia rx'. The 'FPGA' block is labeled '344'.

FIG. 3B is a block diagram of a system architecture. It consists of three main rectangular blocks arranged horizontally. The leftmost block is labeled "Application Specific Accelerators" and is pointed to by reference numeral 358. The middle block is labeled "Internal Memory" and is pointed to by reference numeral 352. The rightmost block is labeled "System Expansion Area" and is pointed to by reference numeral 360. Inside the "System Expansion Area" block, there are three sub-components: "Doorbell" (pointed to by 354), "Vobla Network Processor" (pointed to by 356), and "Peripheral Expansion Area" (pointed to by 350). A curved arrow points from the "Peripheral Expansion Area" towards the "Internal Memory" block.

FIG. 37





204260 "ZEEHOUT"

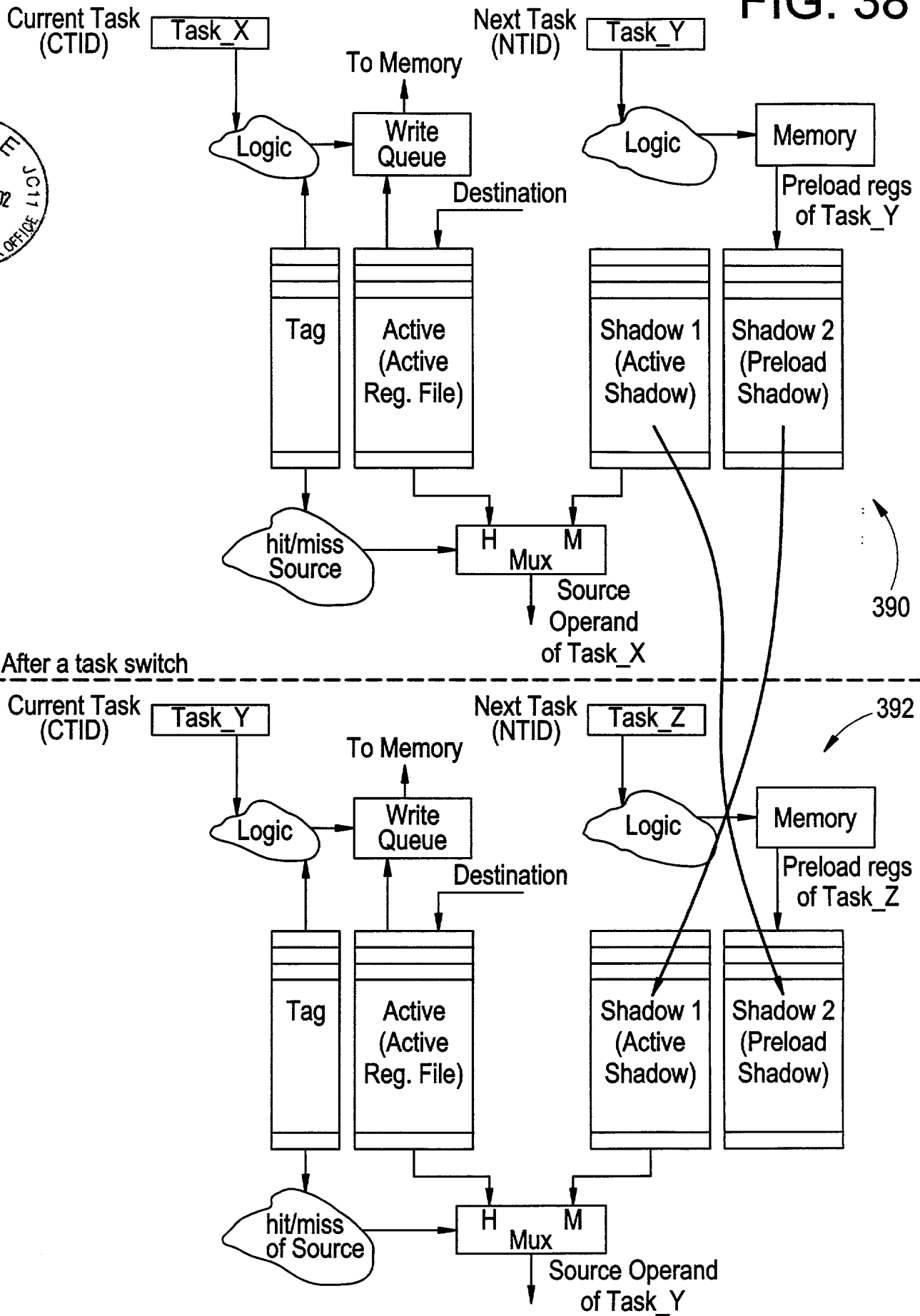


FIG. 39

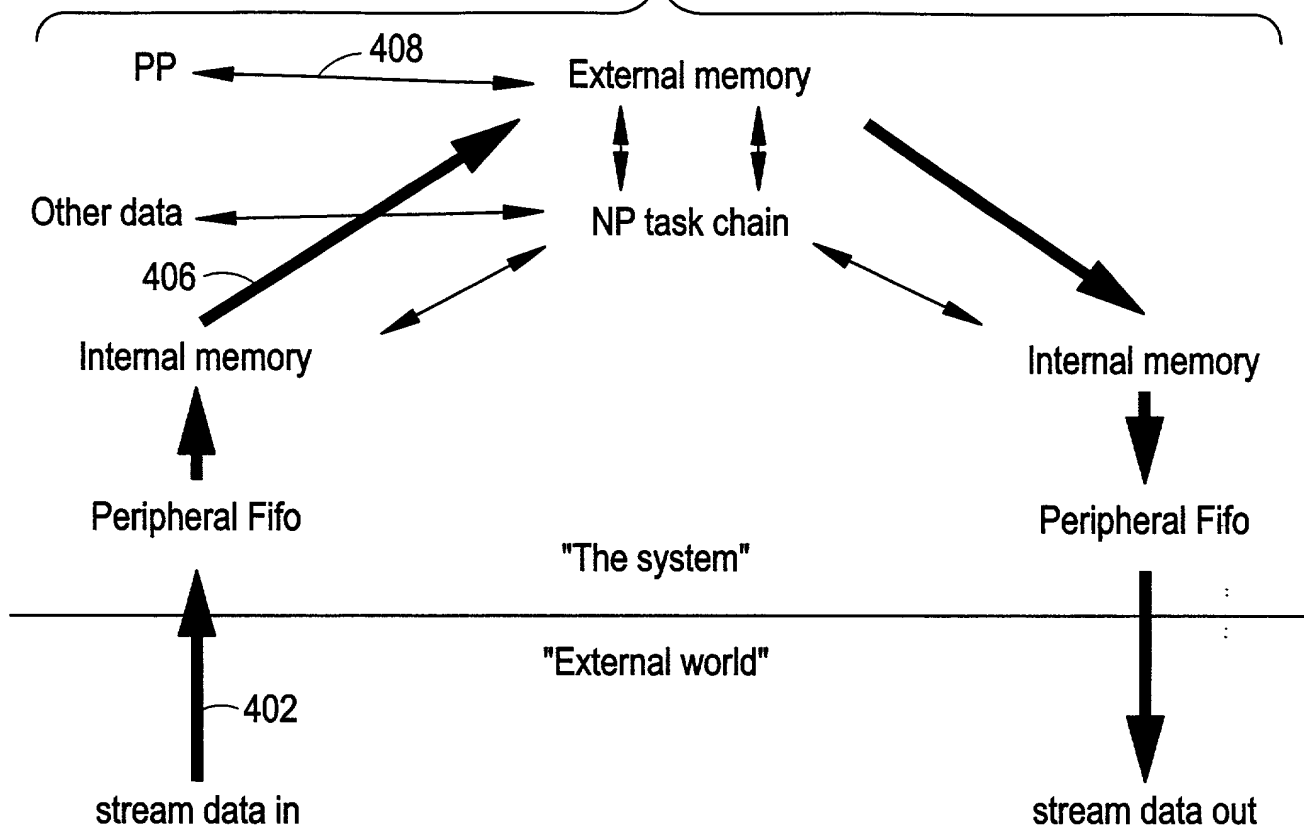


FIG. 40

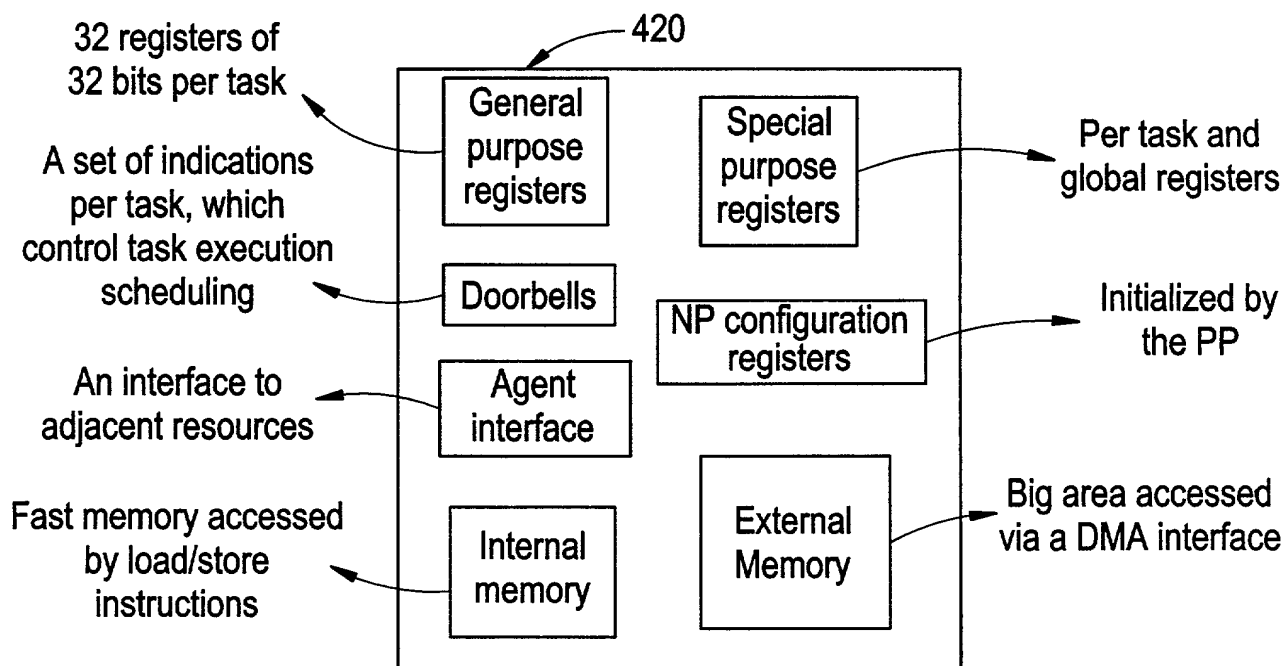
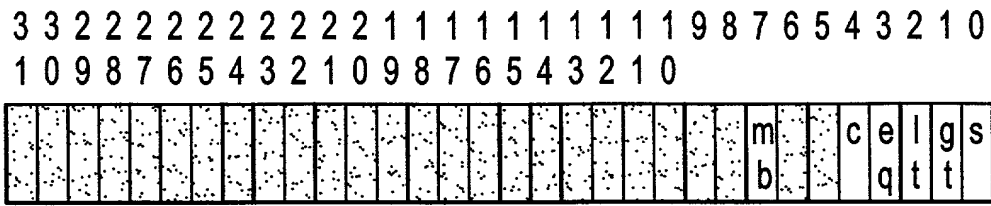


FIG. 41

R1 register

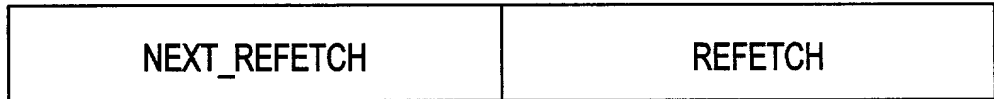


s - sticky bit
 eq - equal/zero
 lt - less then/negative
 gt - greater then/positive
 c - carry
 mb - reflection of the RAM mult-reader busy indication

430

FIG. 42

REFETCH SPR
(spr index - 0)



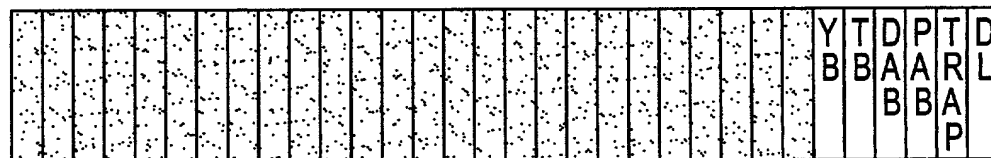
440

TASK SPR
(spr index - 1)



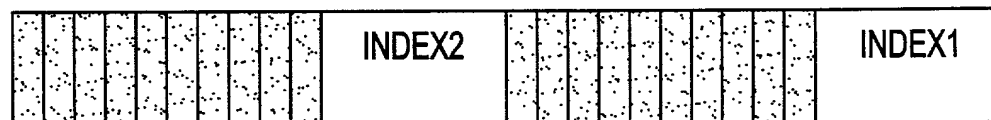
442

TRAP SPR
(spr index - 2)



444

MINDEX SPR
(spr index - 3)



446

FIG. 43

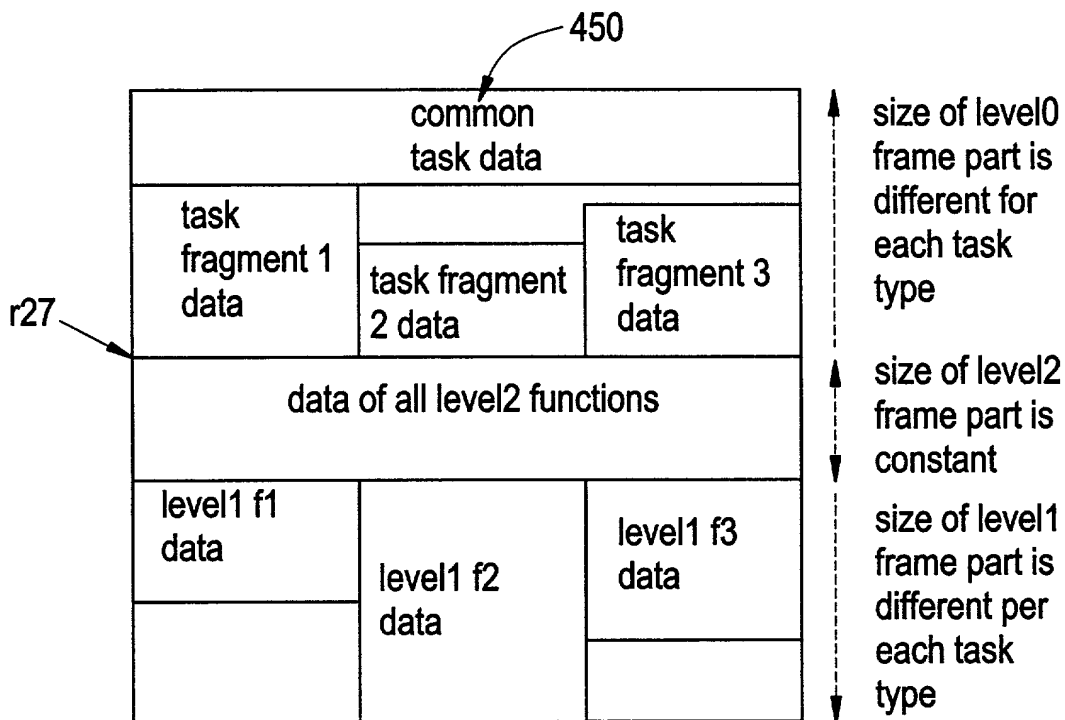


FIG. 44

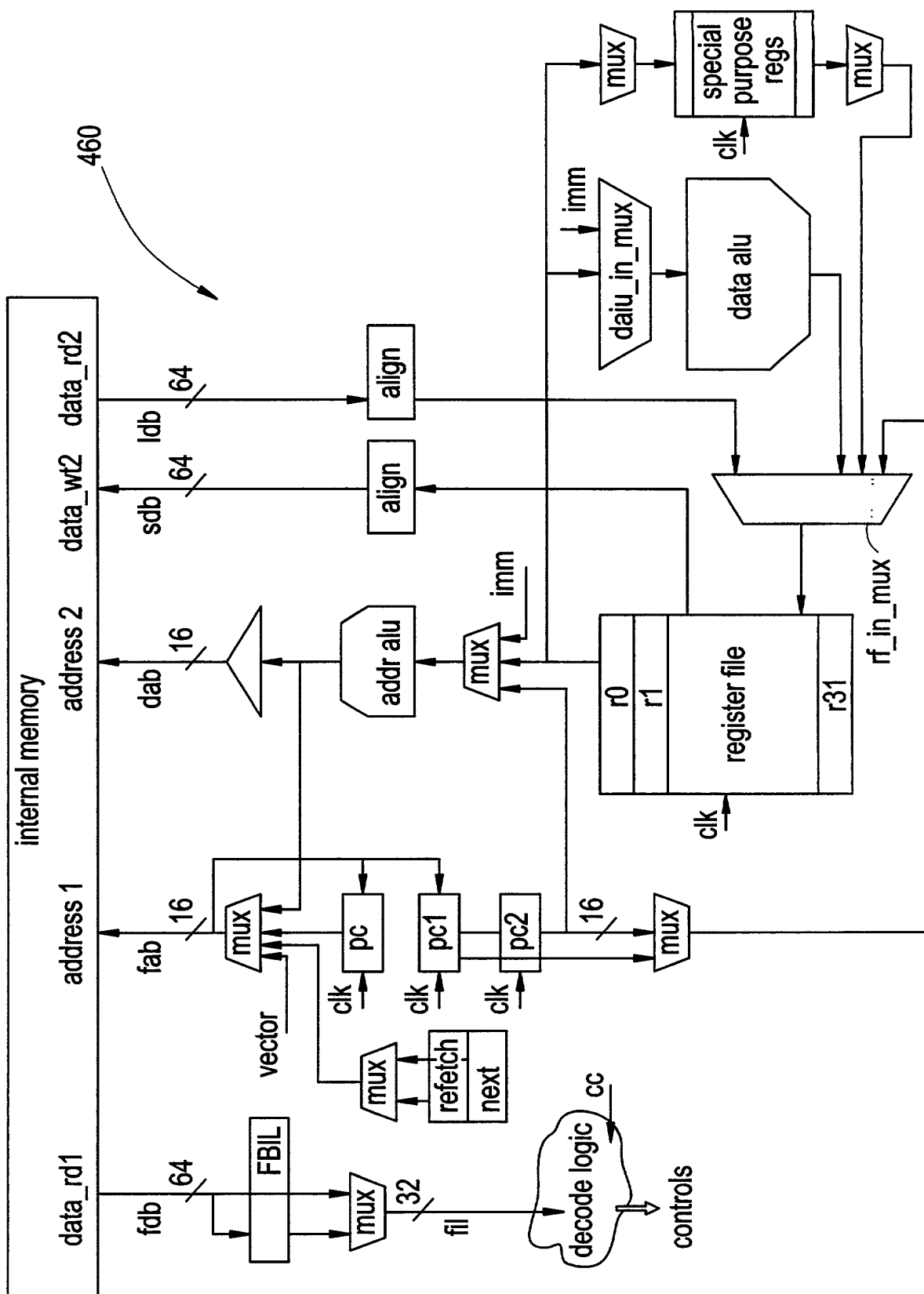
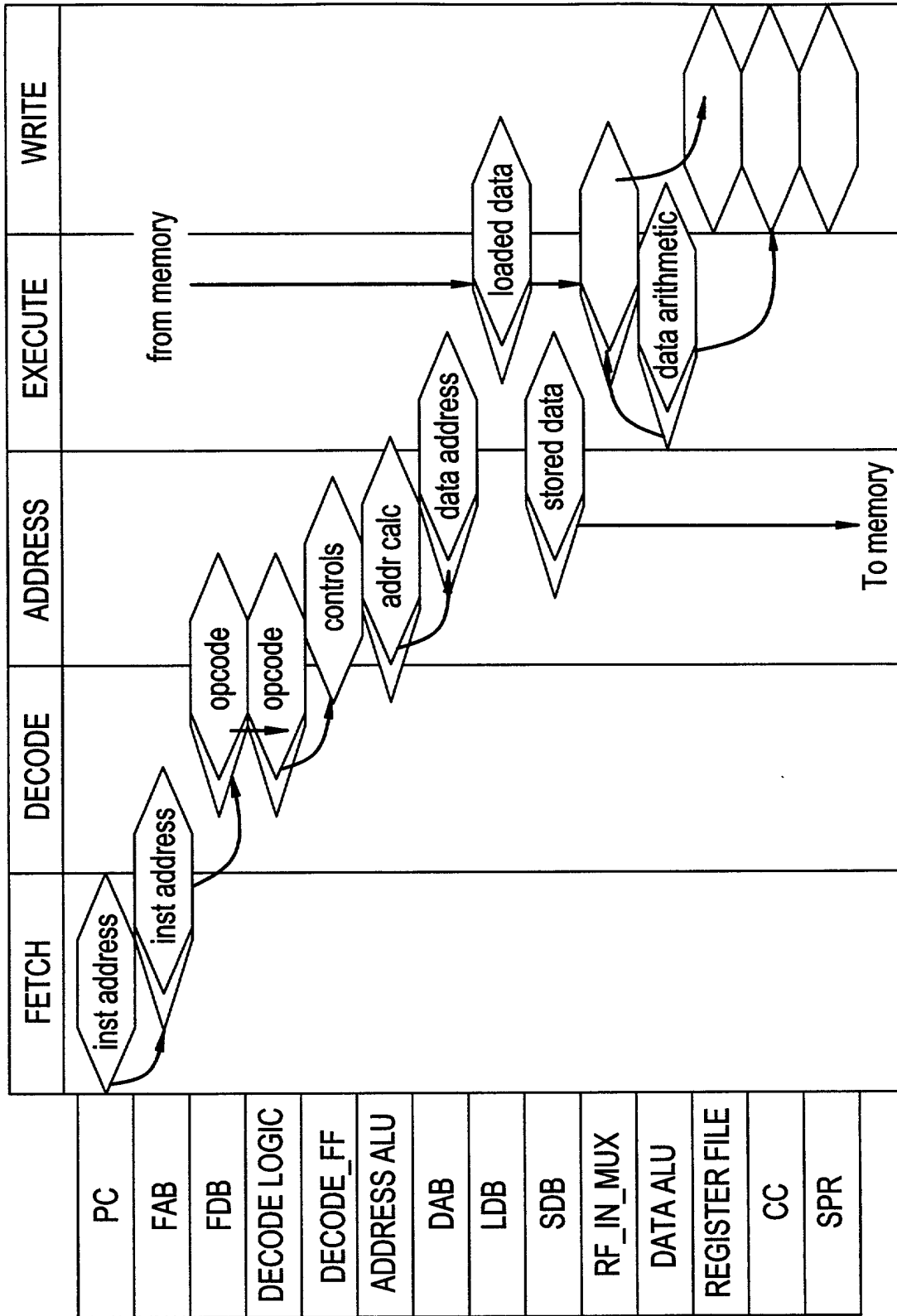


FIG. 45



 - Flip Flop
  - Logic

FIG. 46

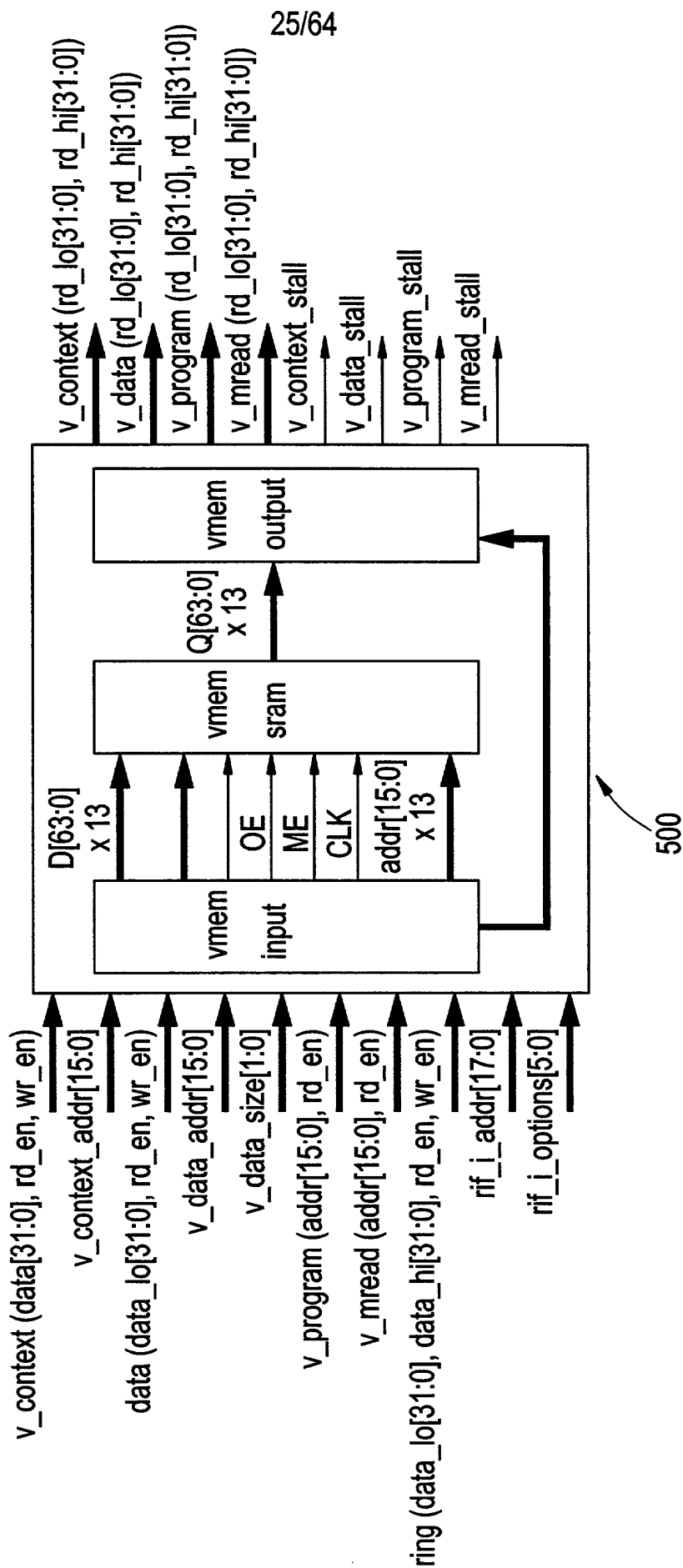


FIG. 47

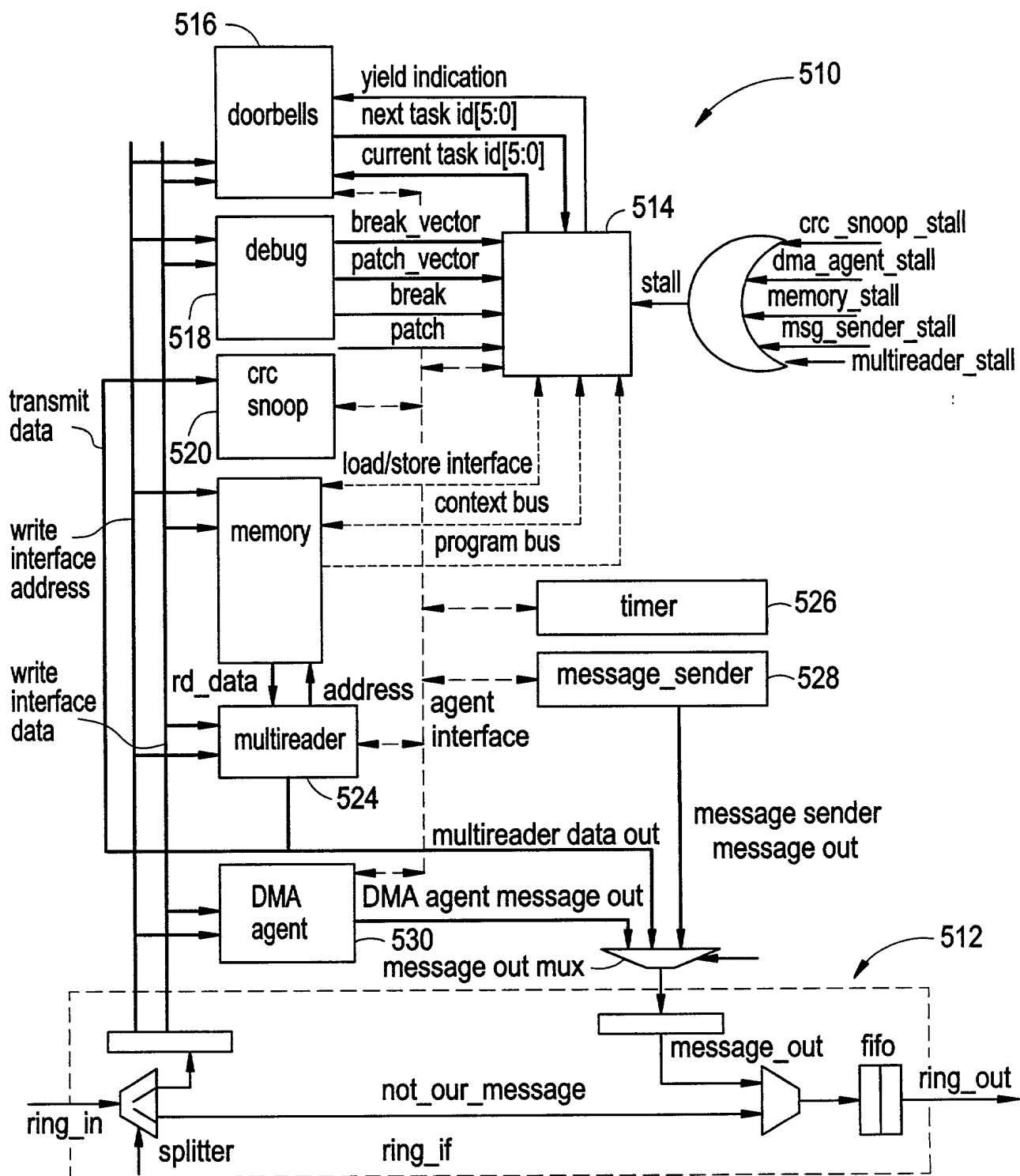


FIG. 48

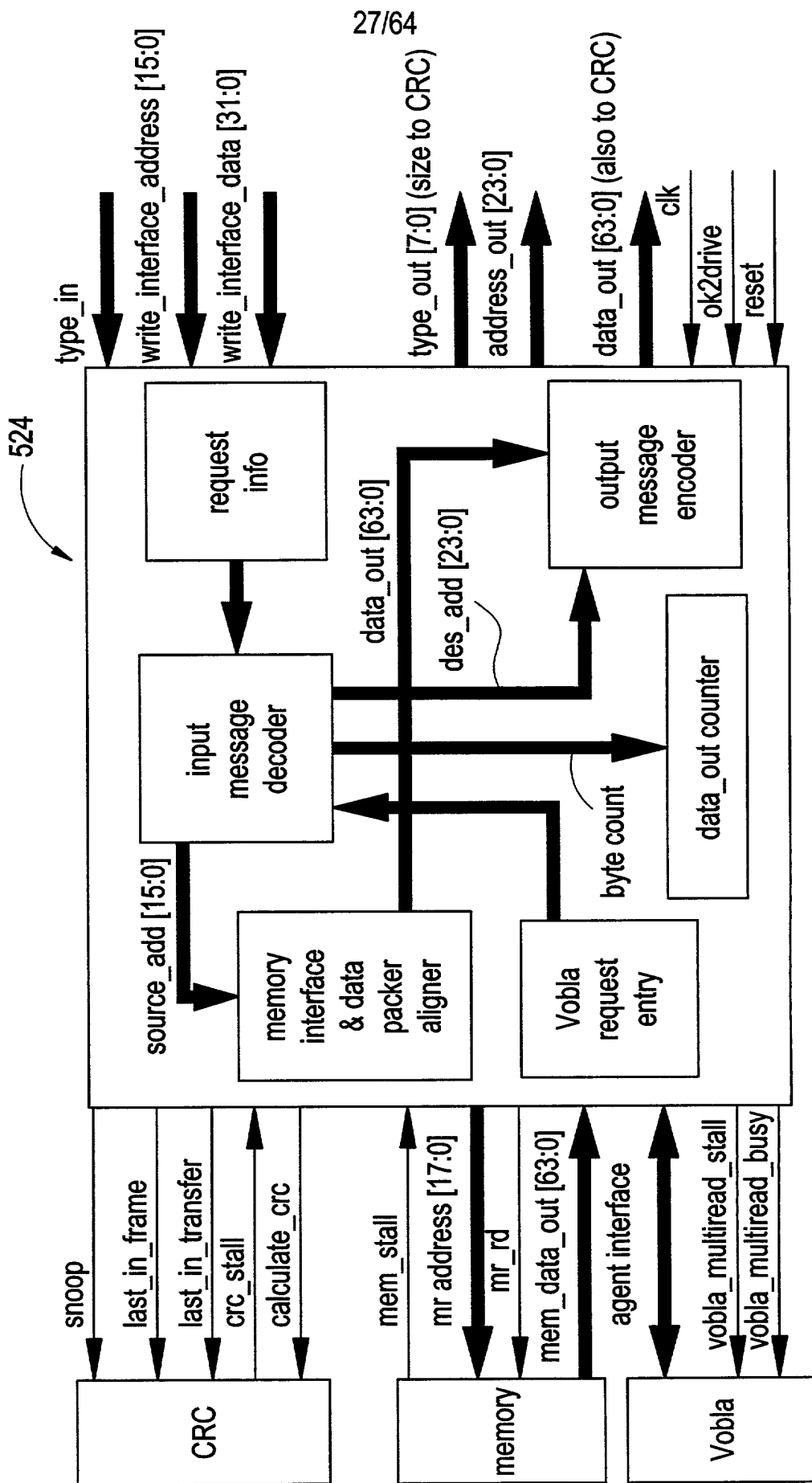


FIG. 49

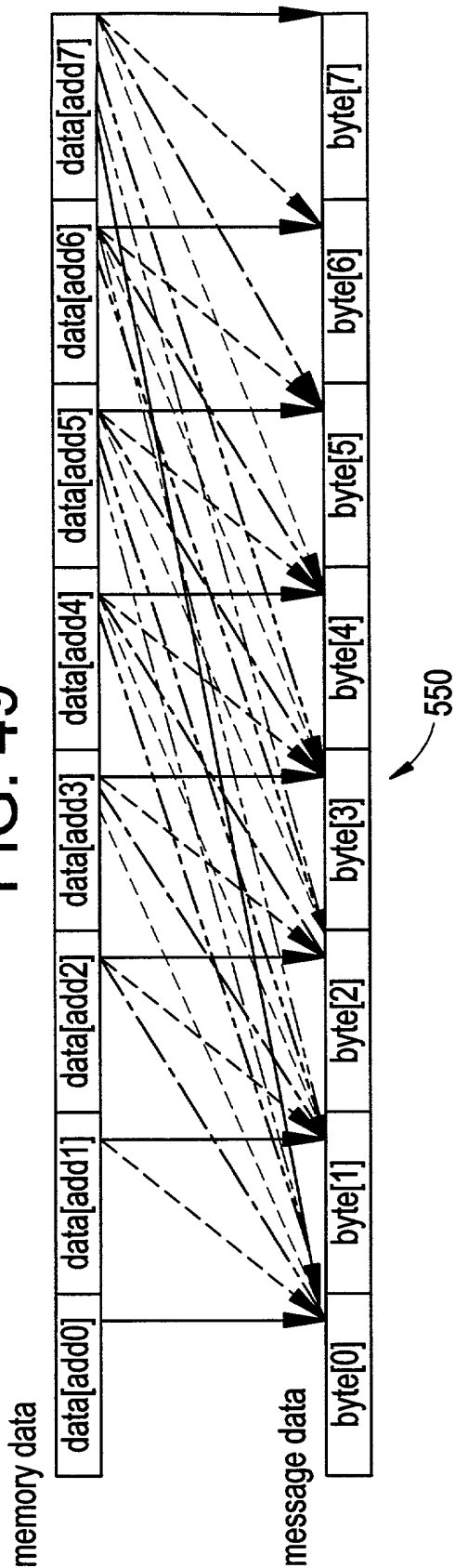
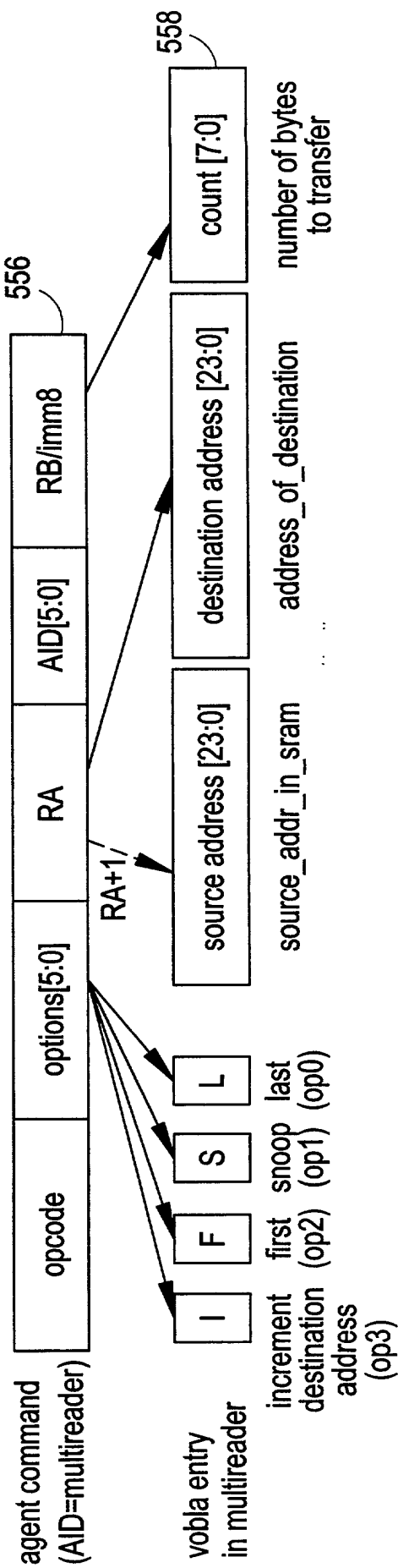


FIG. 50



204260" 4664300T

FIG. 51

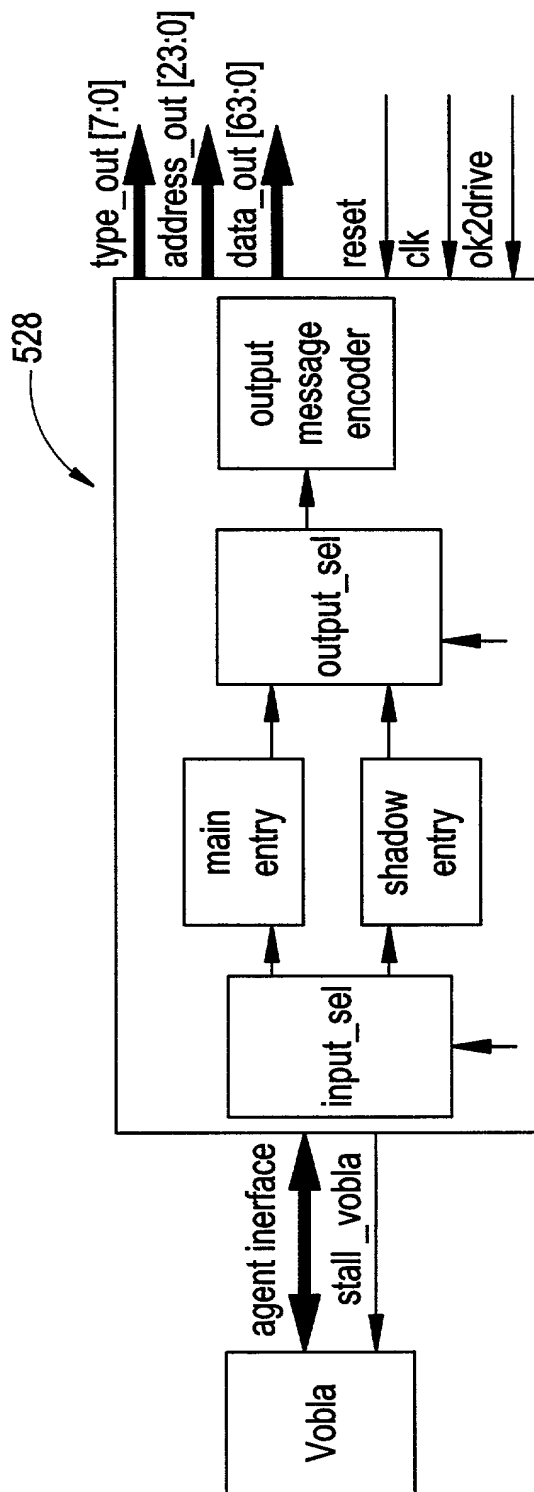


FIG. 52

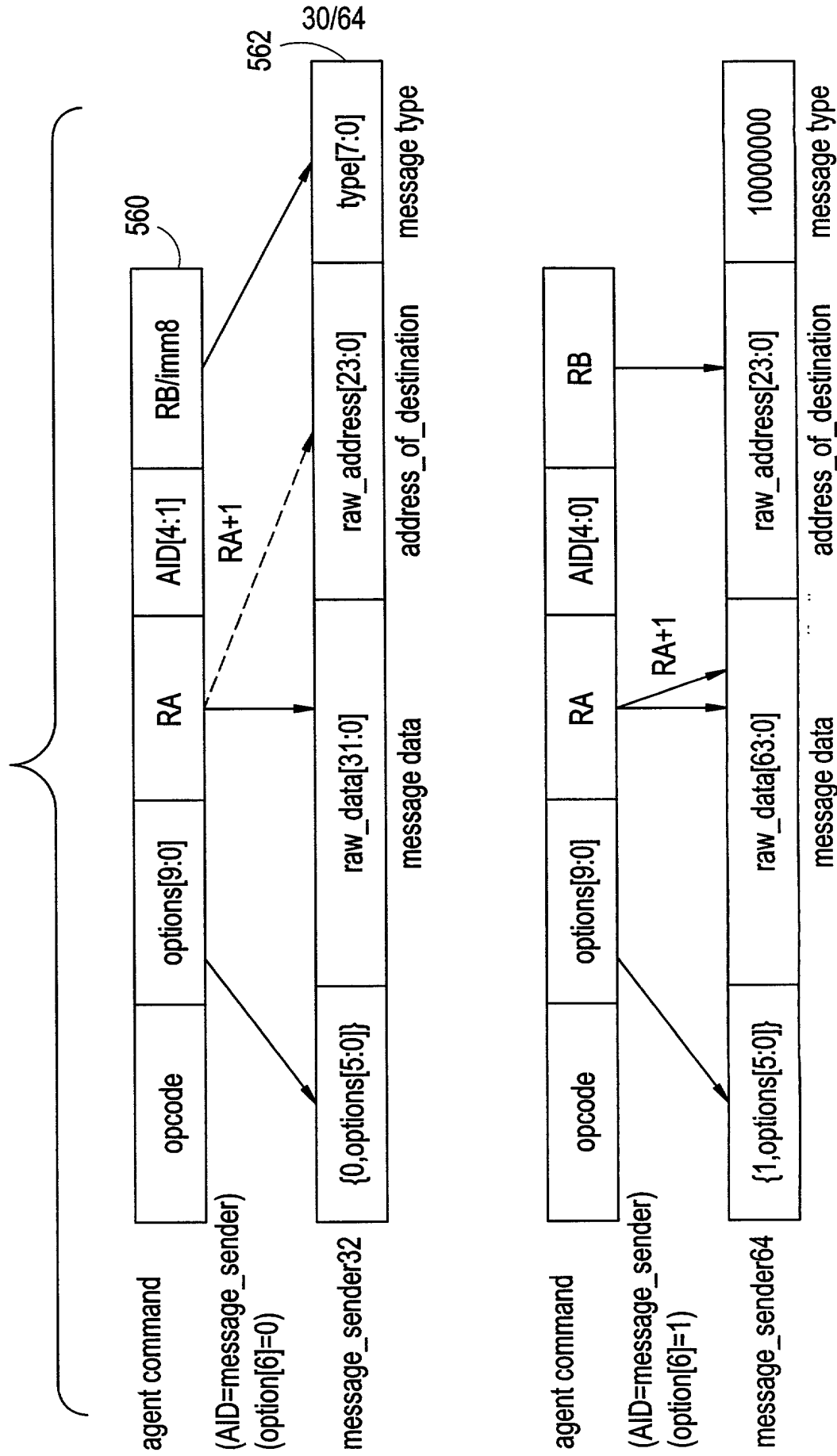


FIG. 53

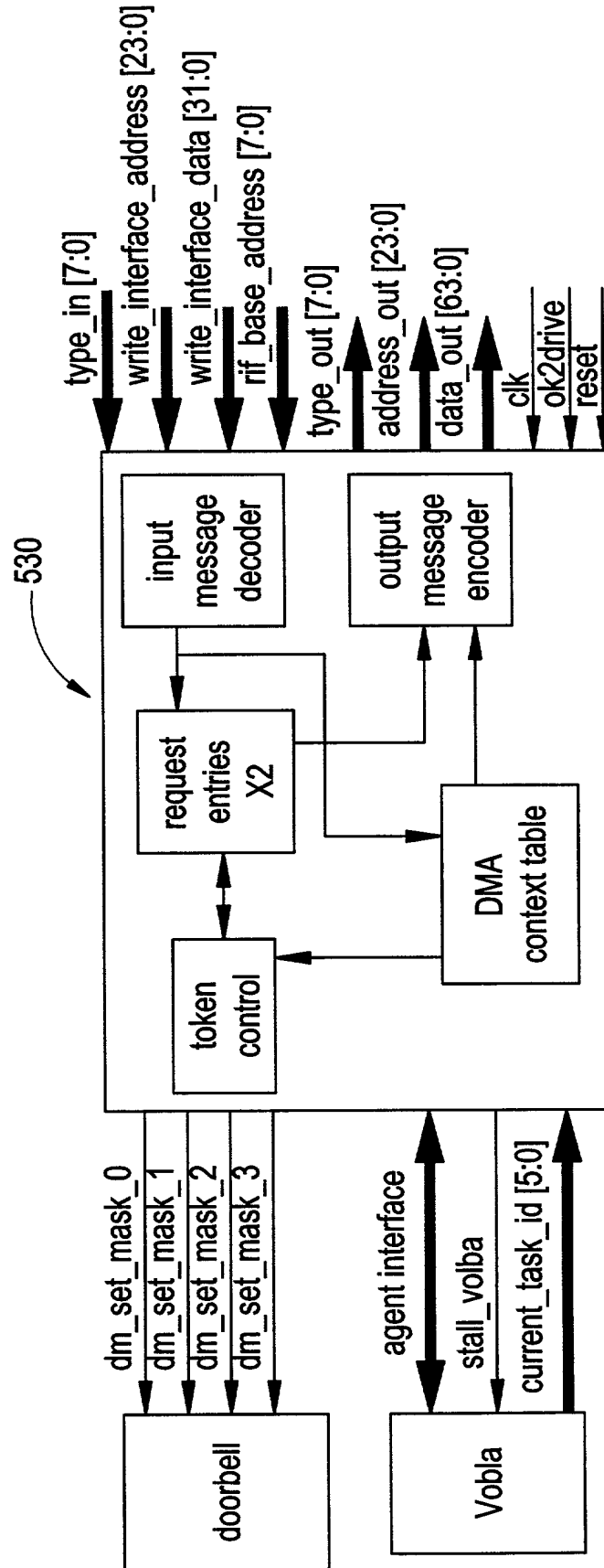


FIG. 54

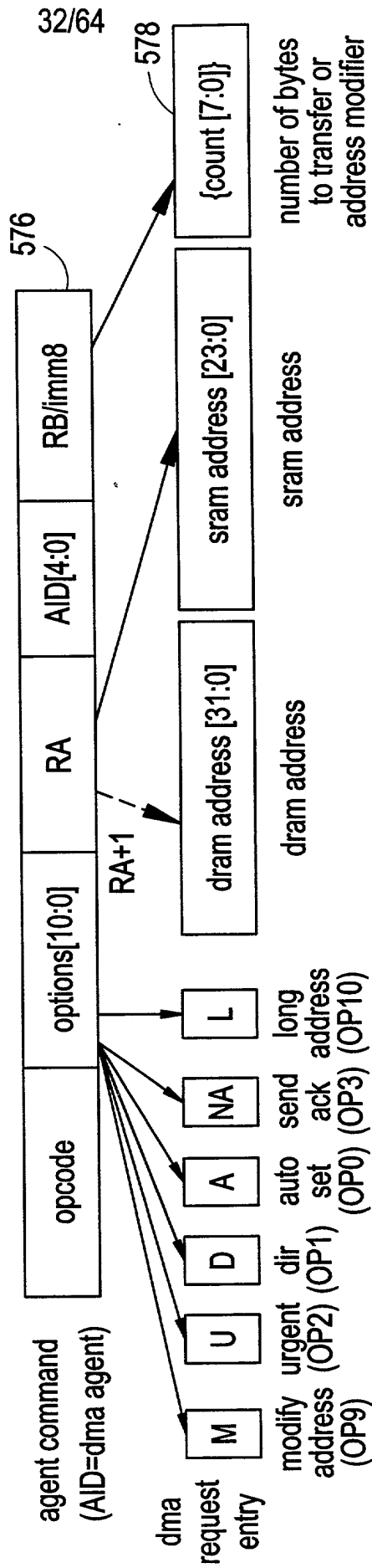


FIG. 55

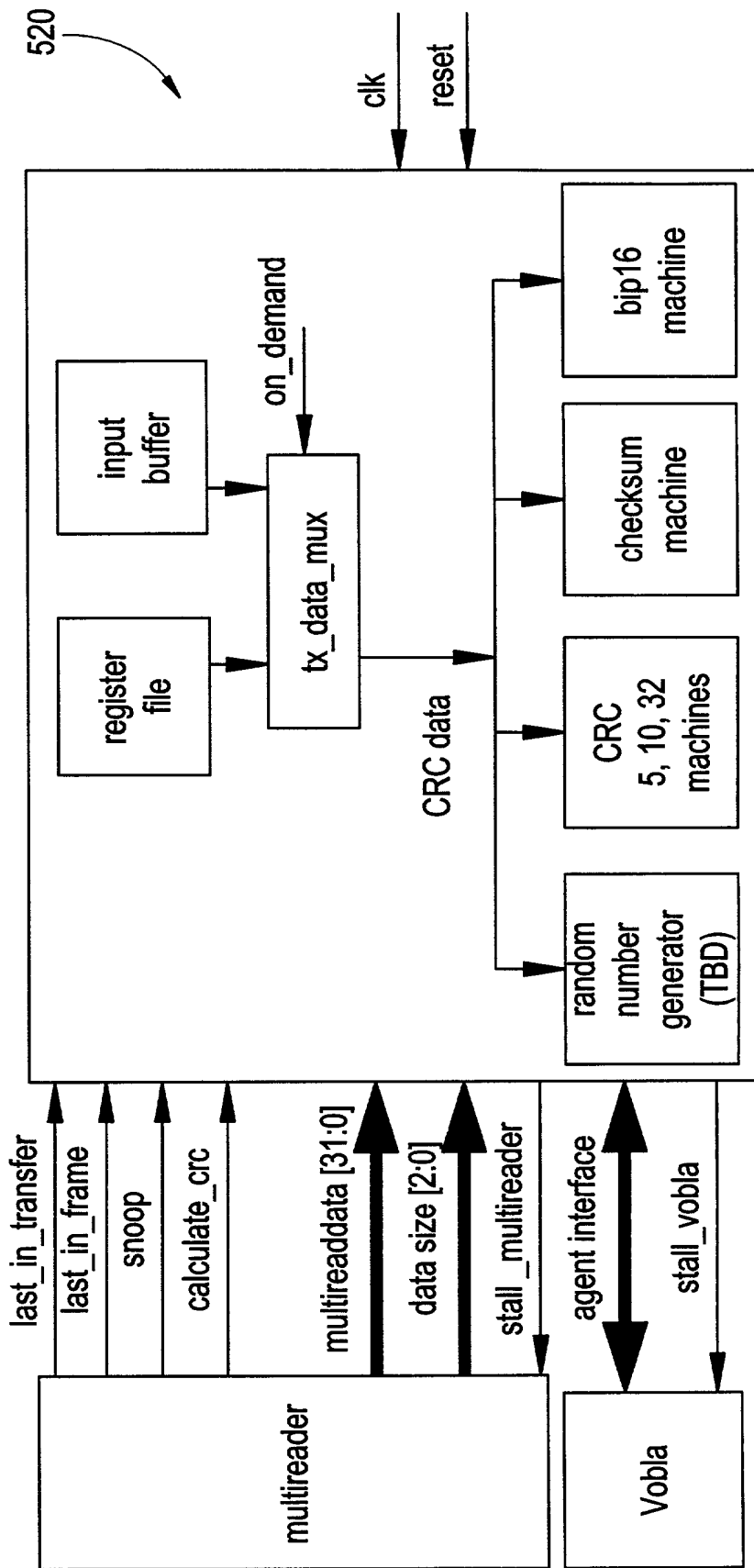


FIG. 56

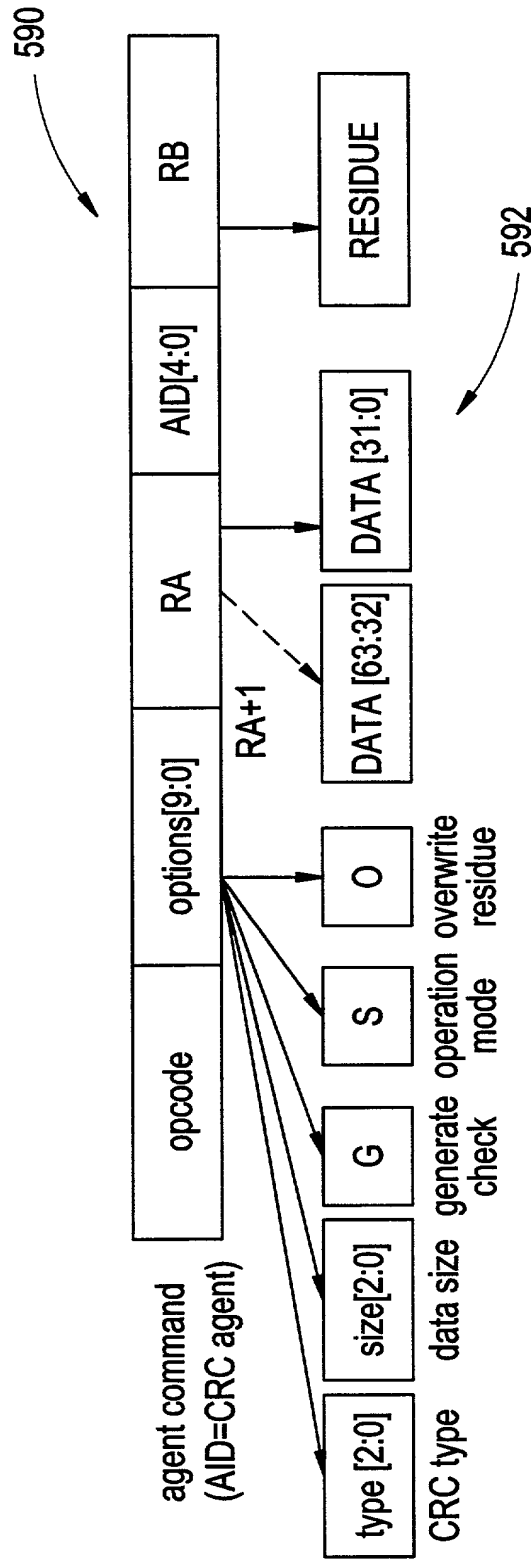


FIG. 57

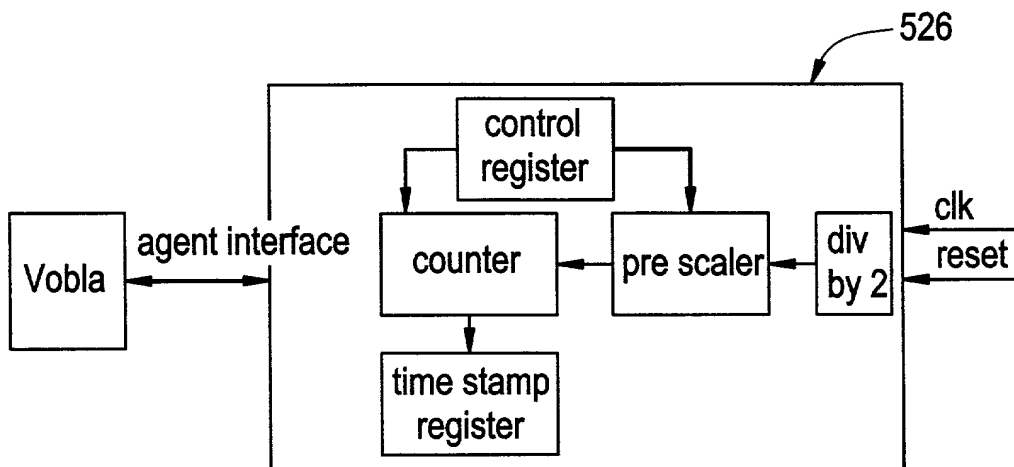


FIG. 58

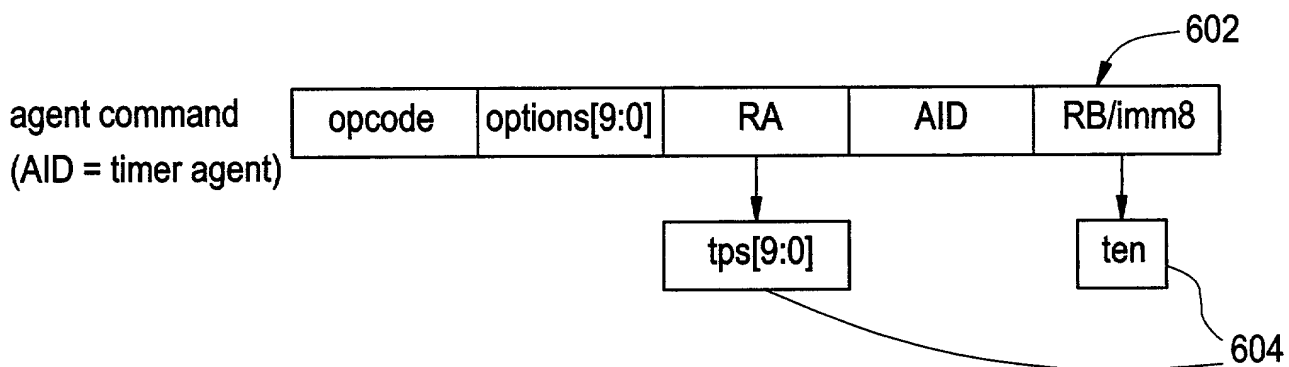


FIG. 59

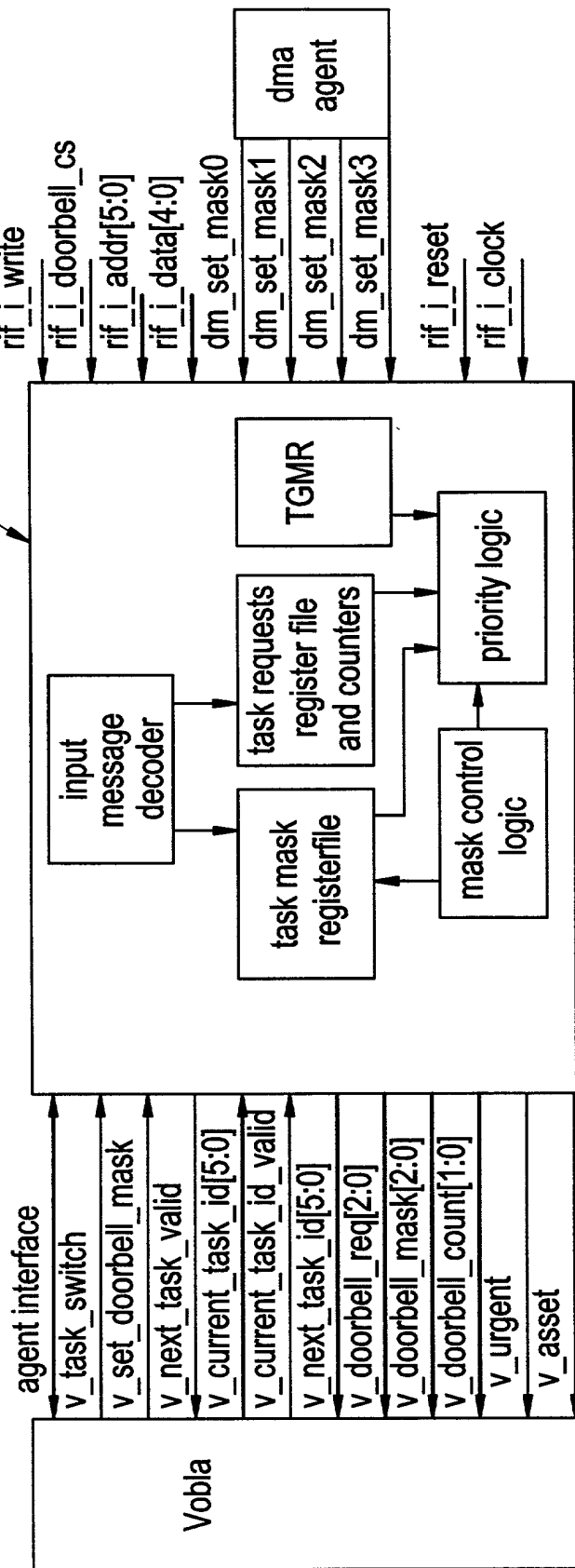


FIG. 60

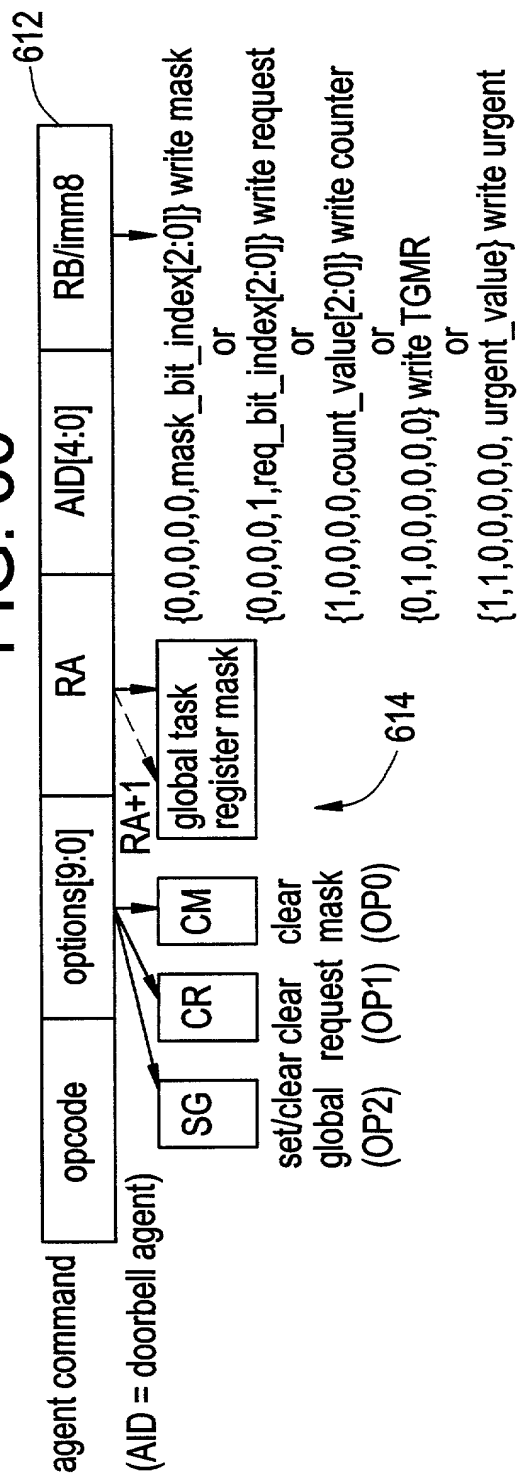


FIG. 61

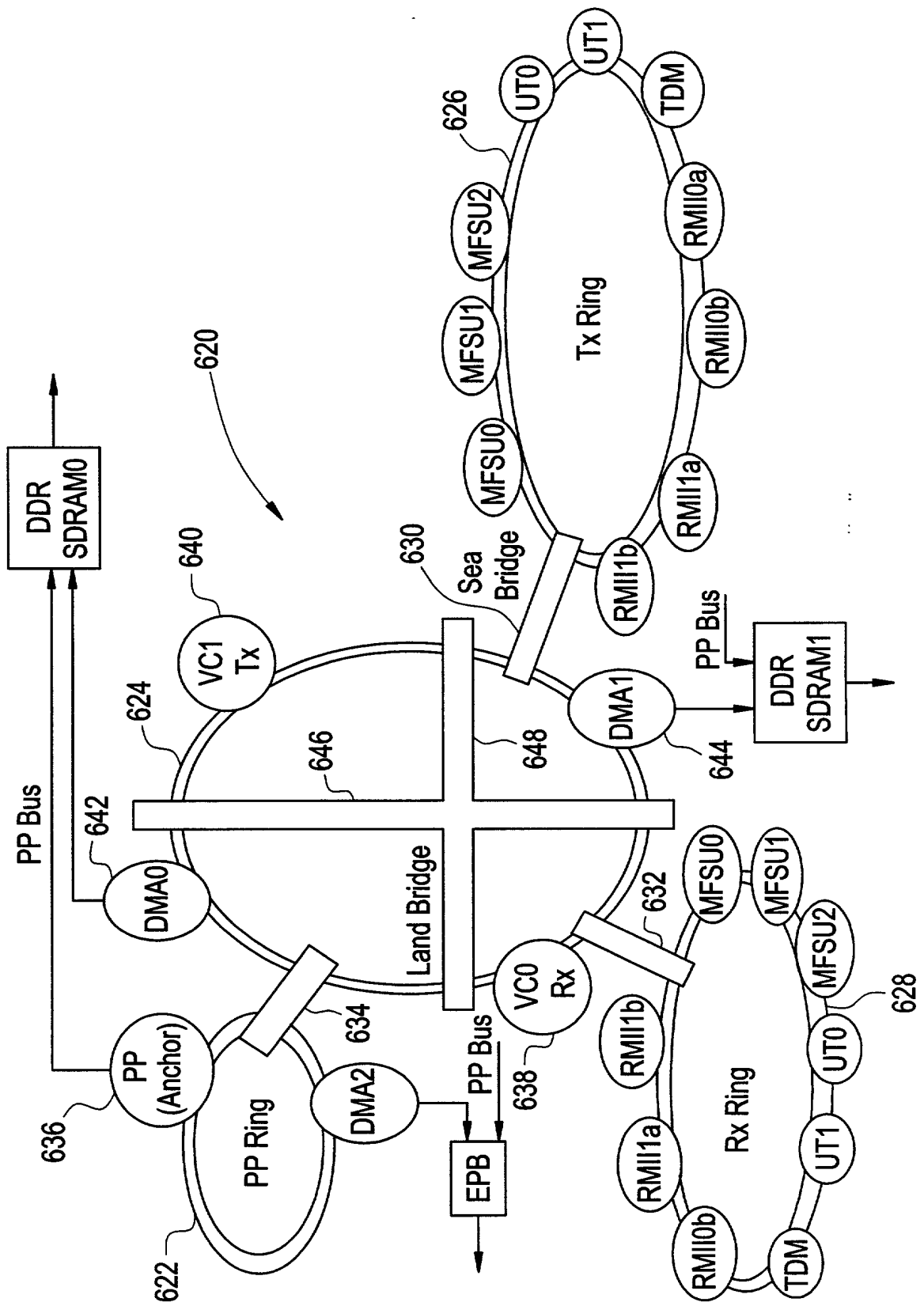


FIG. 62

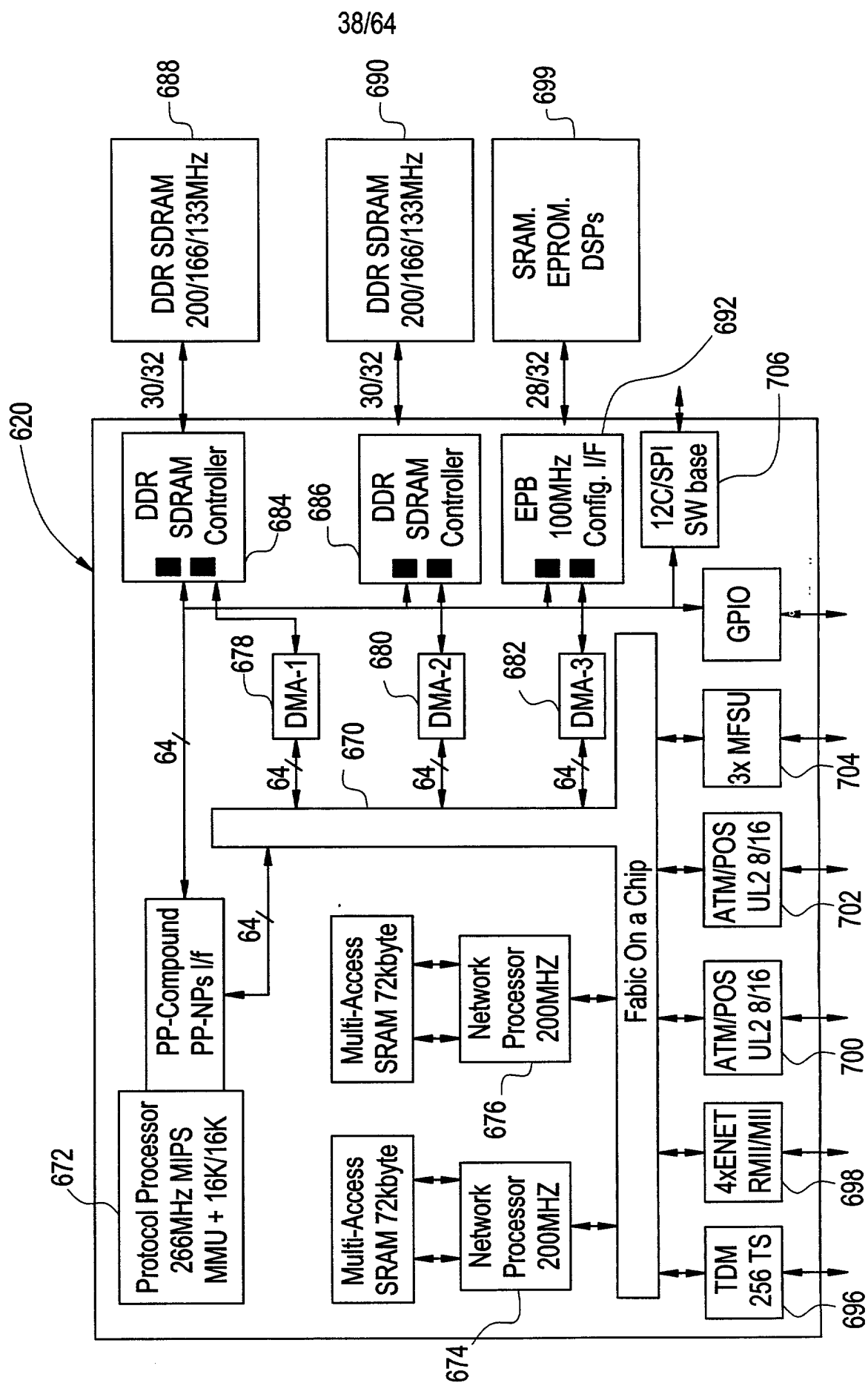


FIG. 63

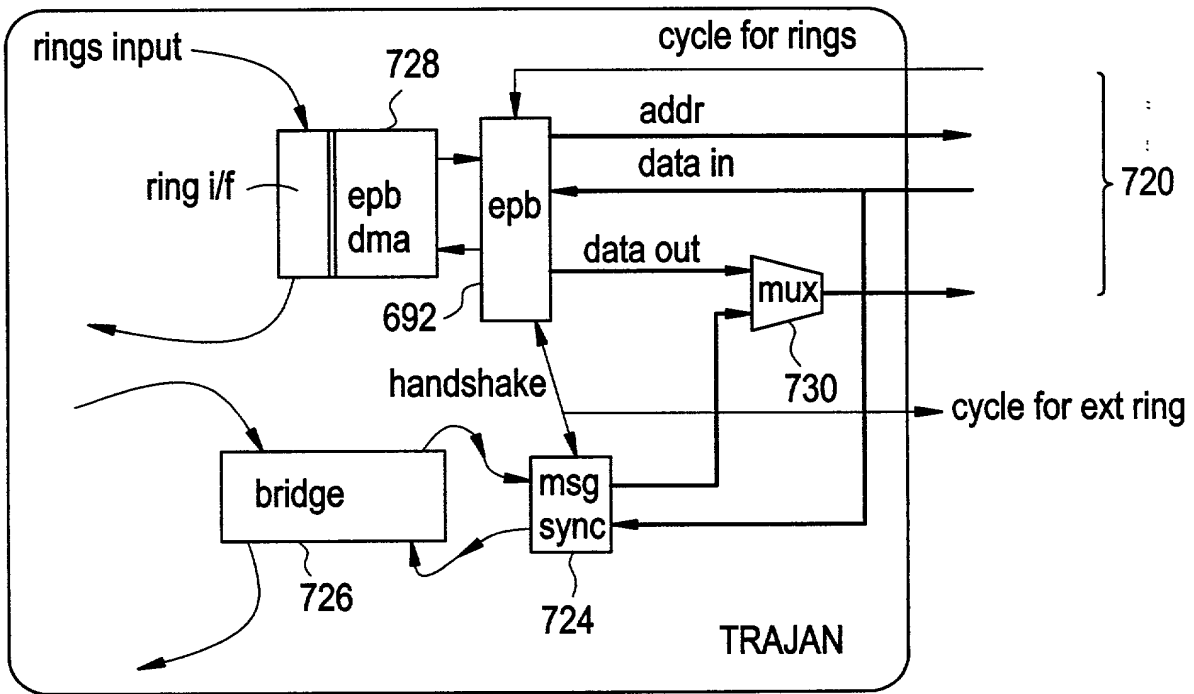


FIG. 64

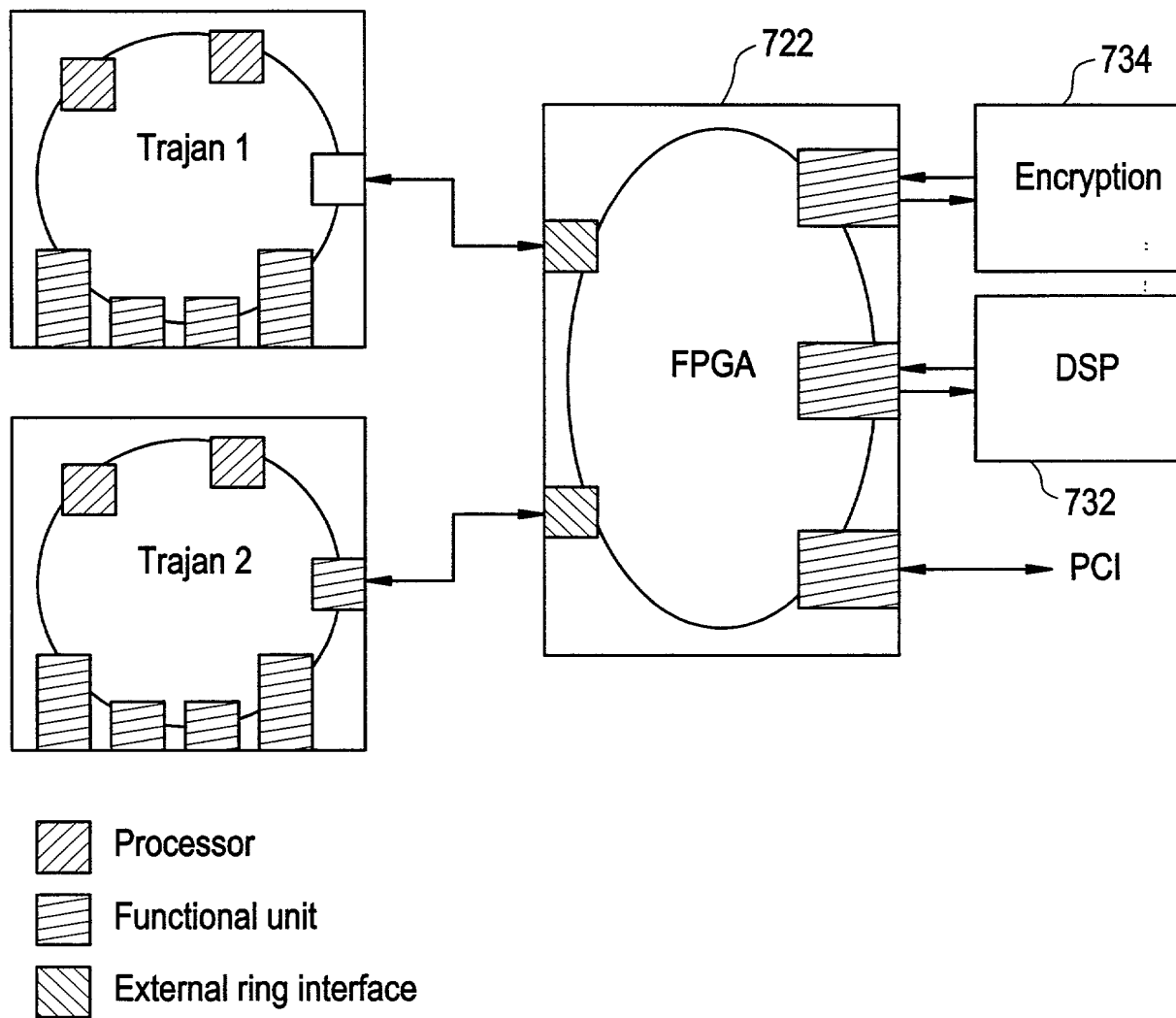


FIG. 65

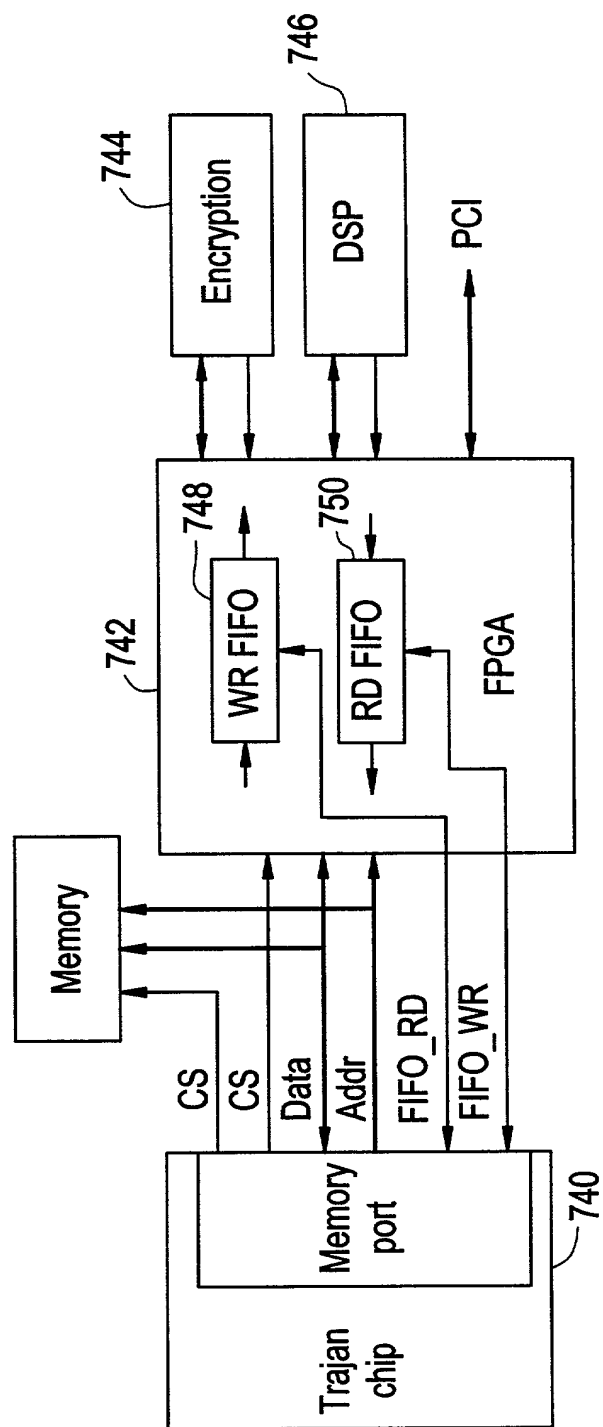


FIG. 66

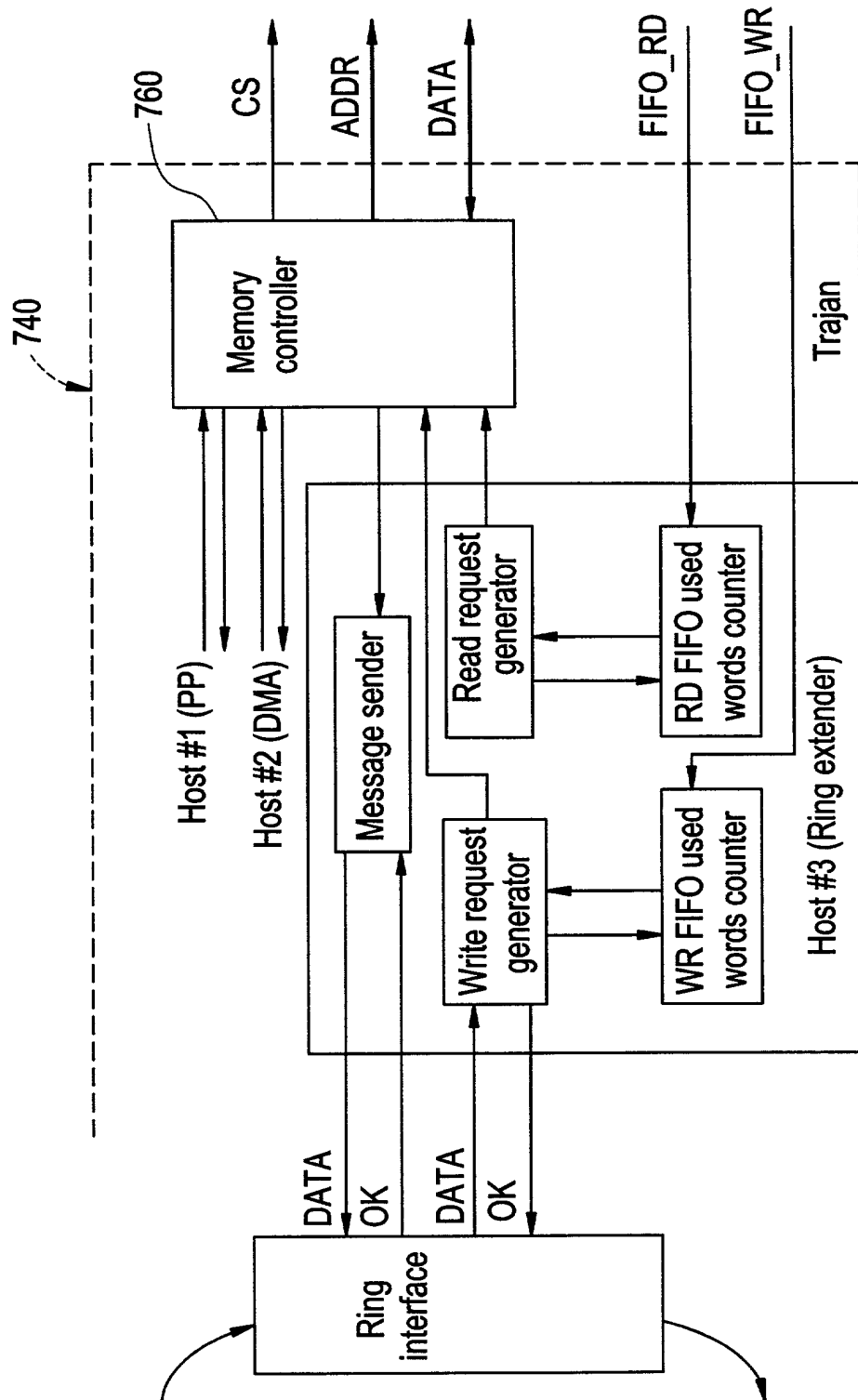


FIG. 67

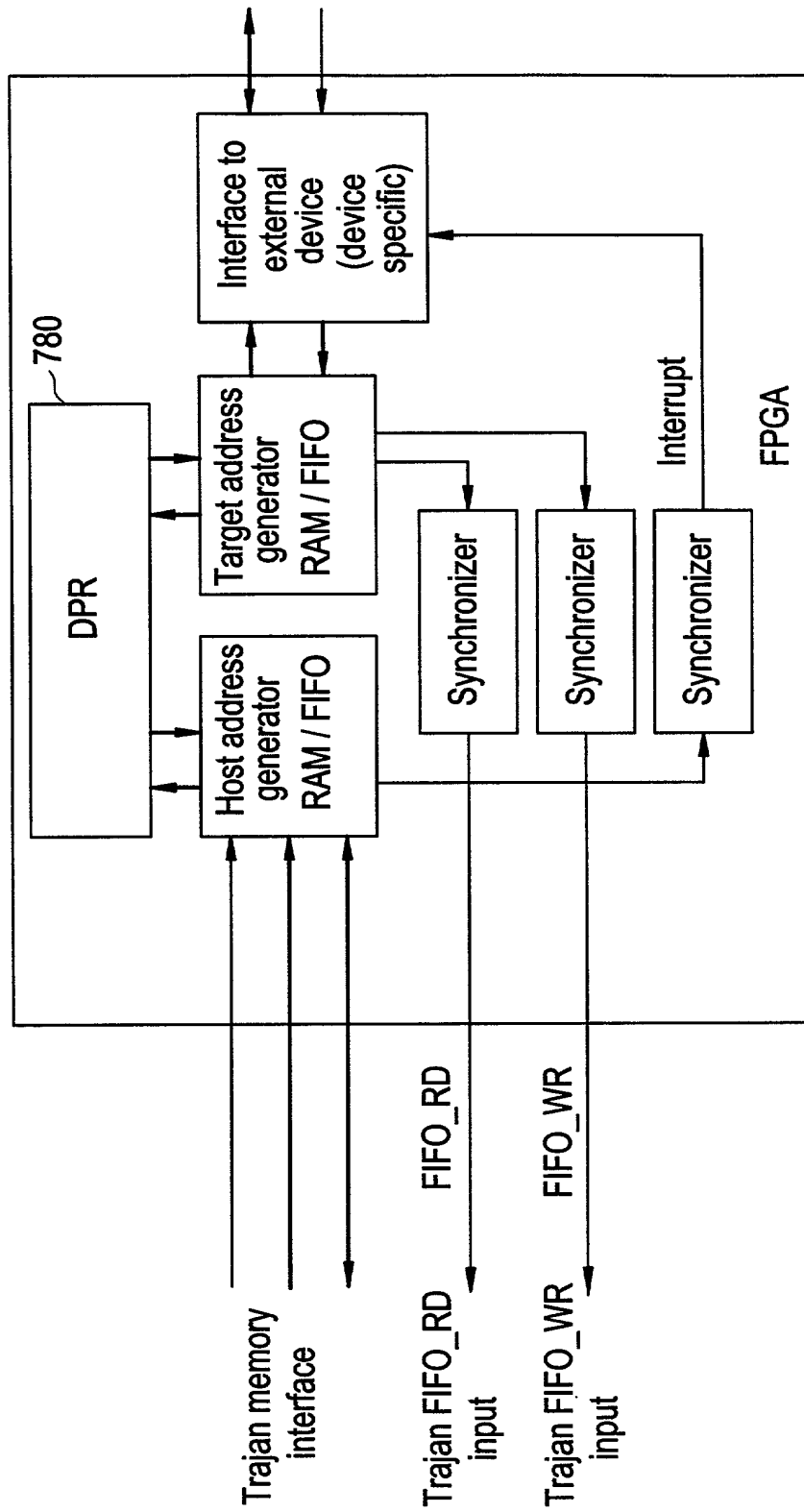


FIG. 68

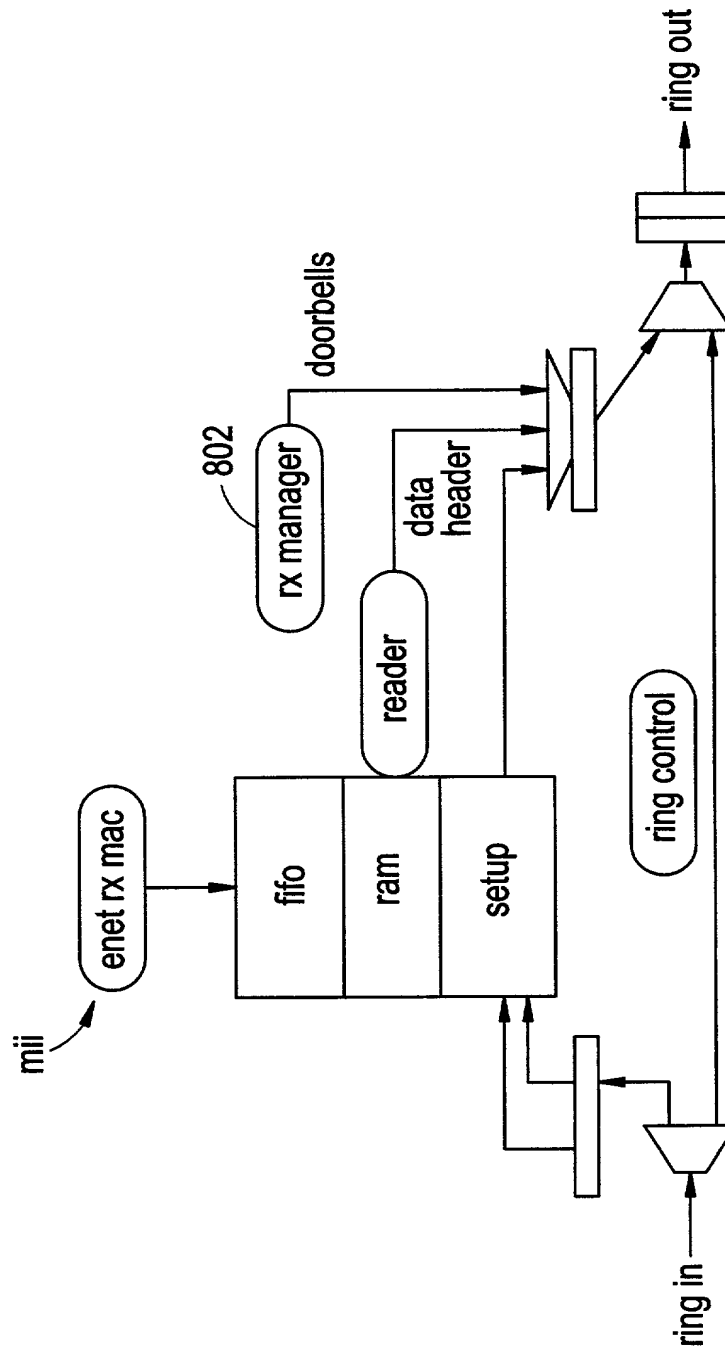


FIG. 69

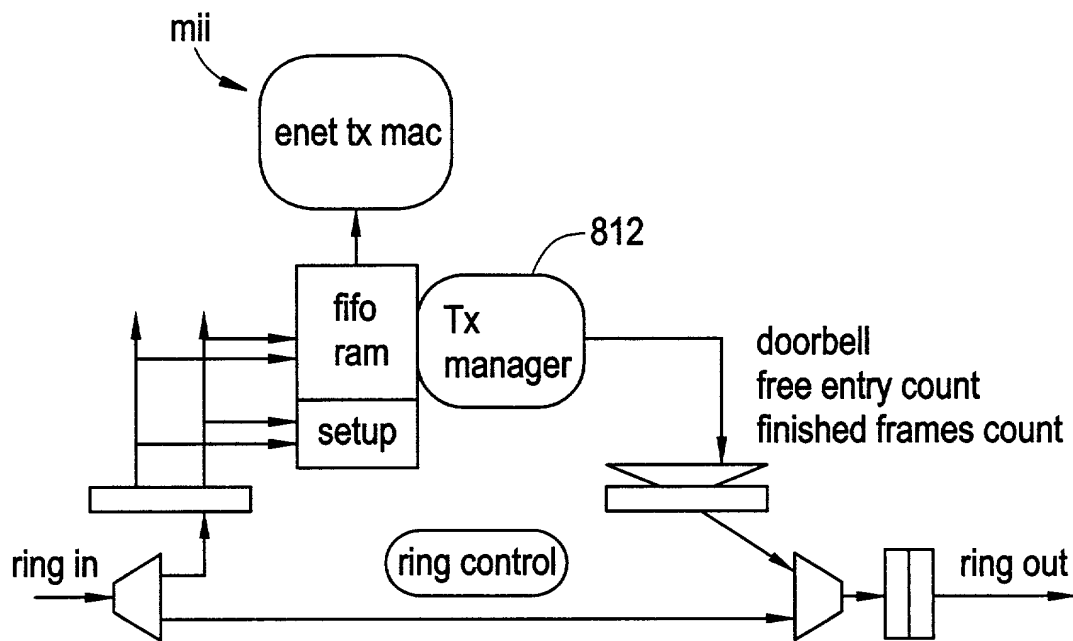


FIG. 70

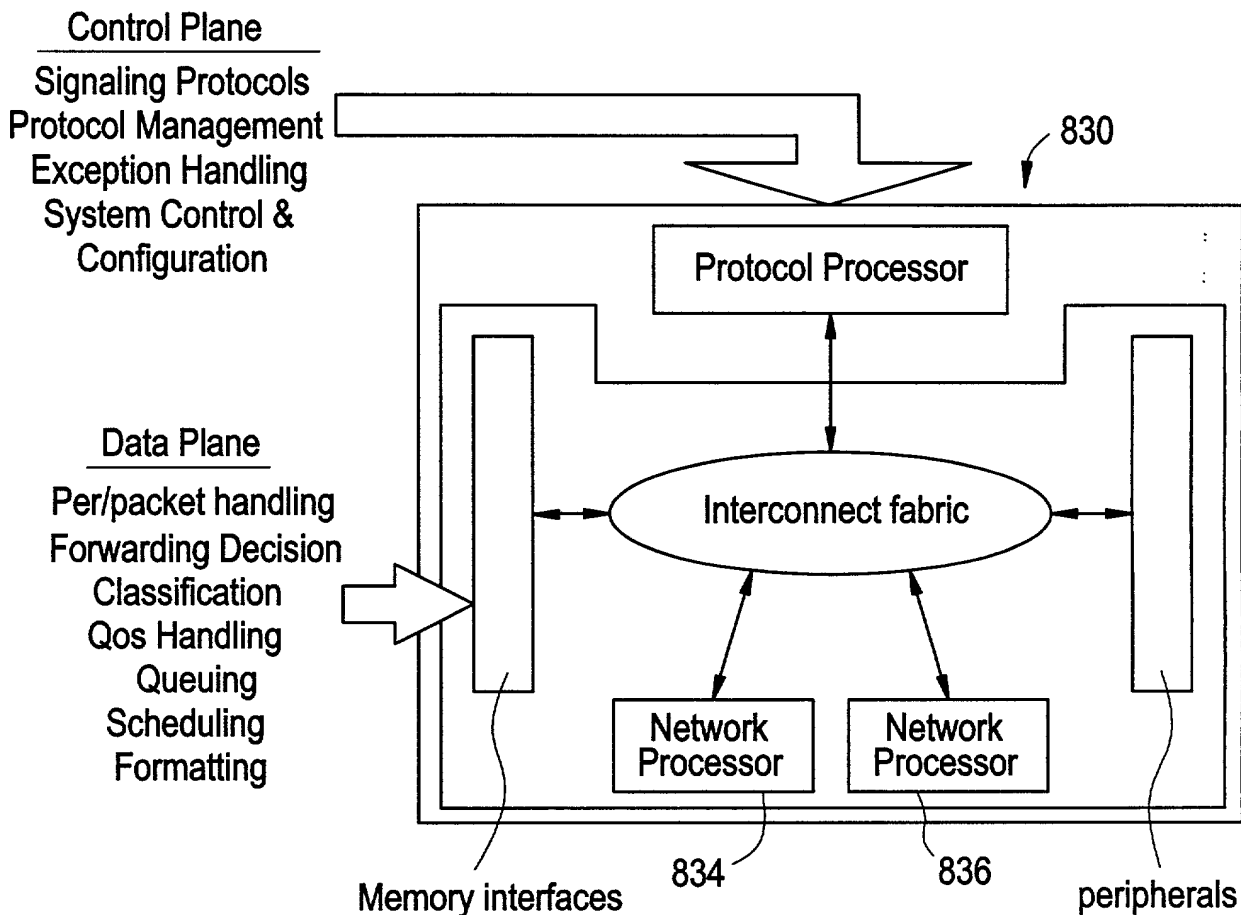


FIG. 71

840

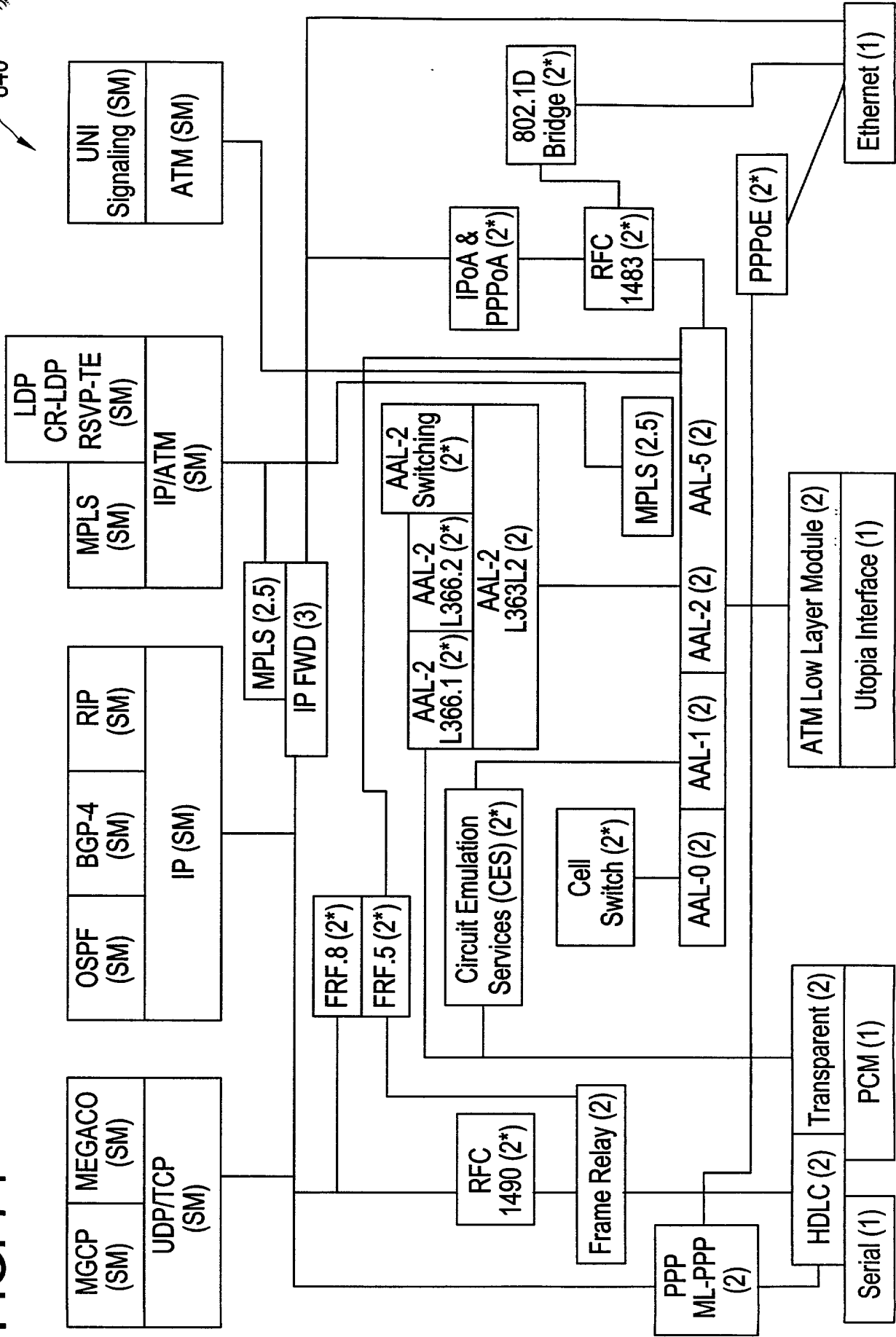
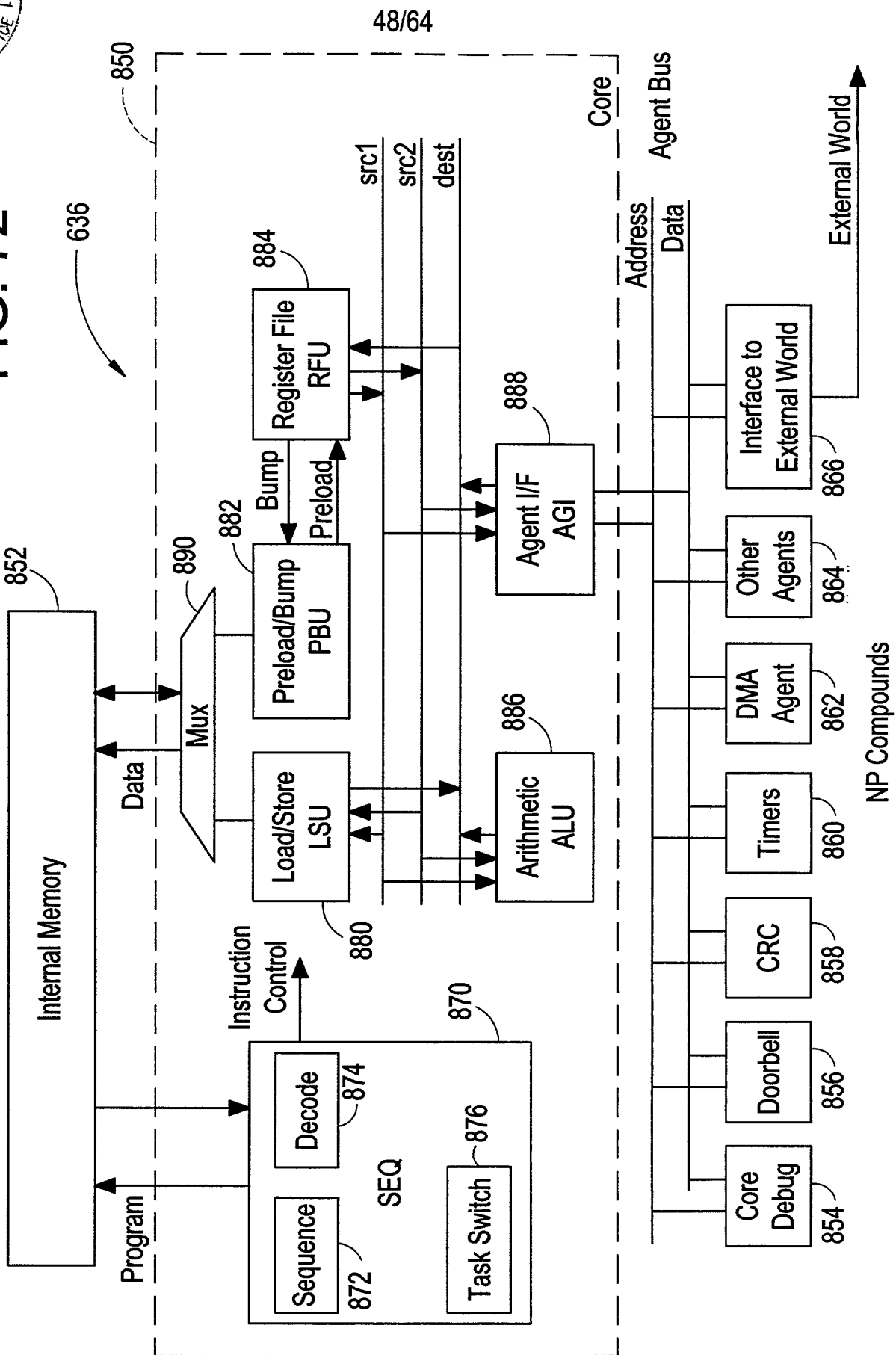




FIG. 72



20020924

FIG. 73

900

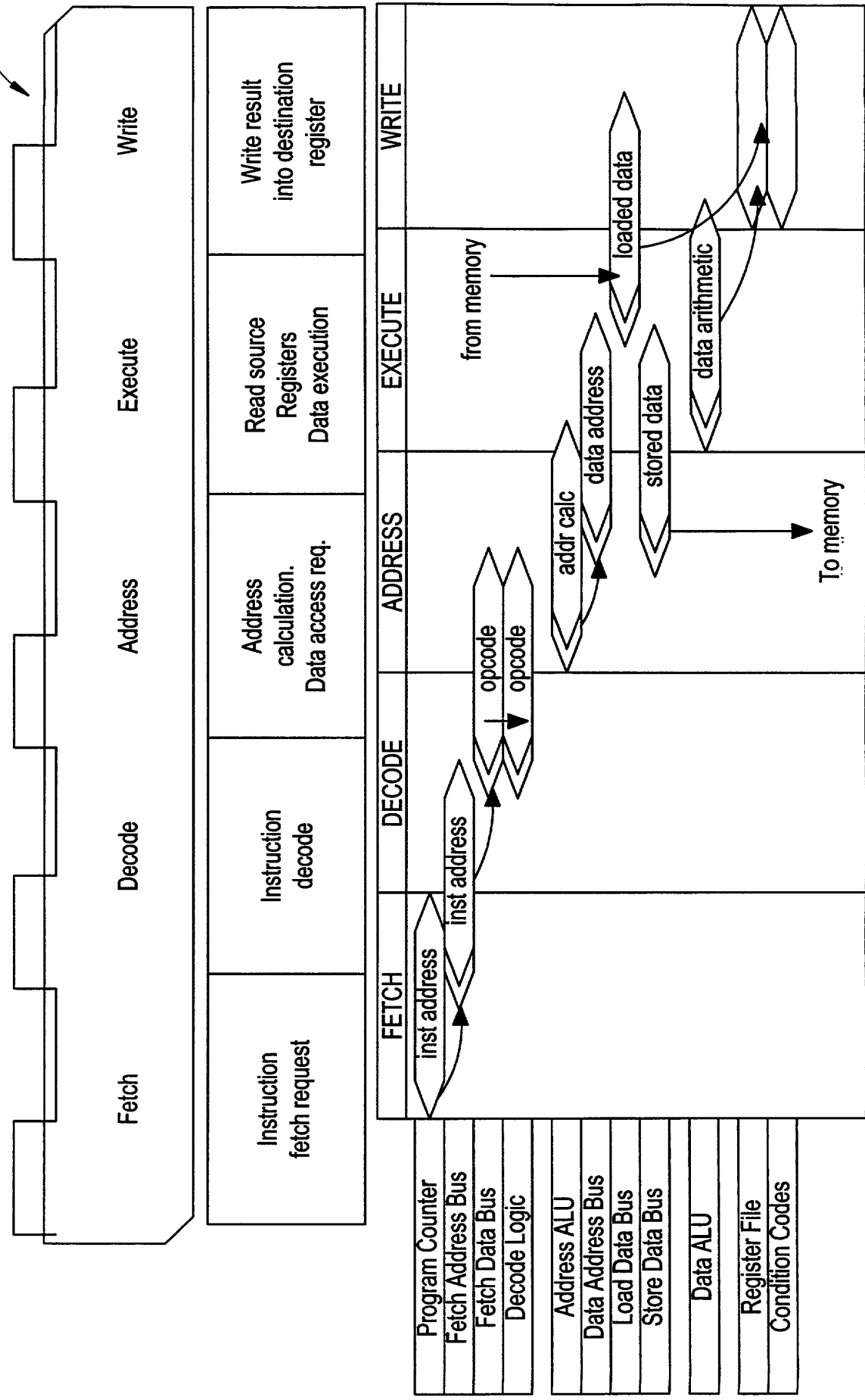


FIG. 74

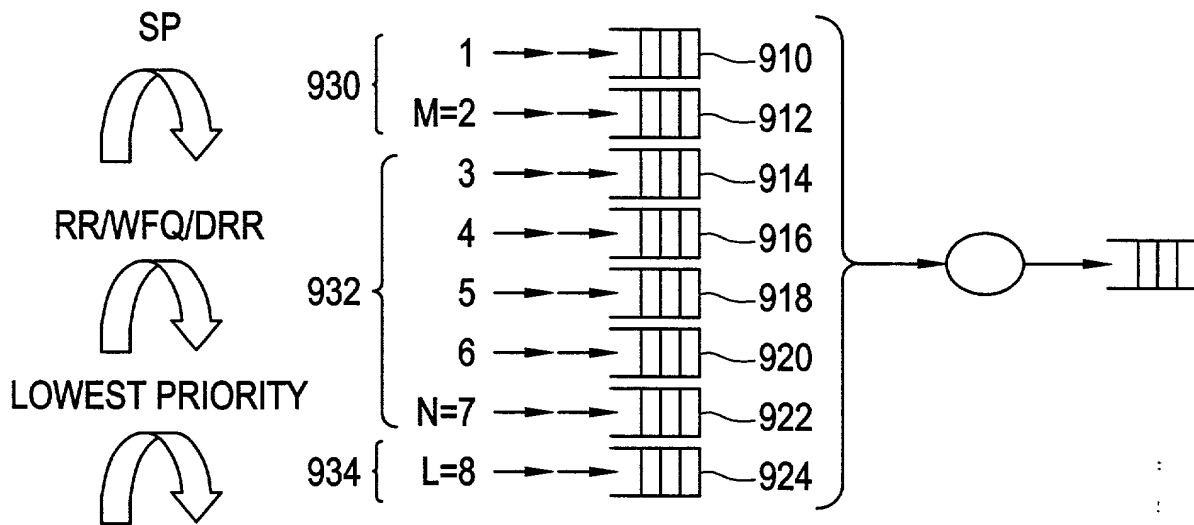


FIG. 75

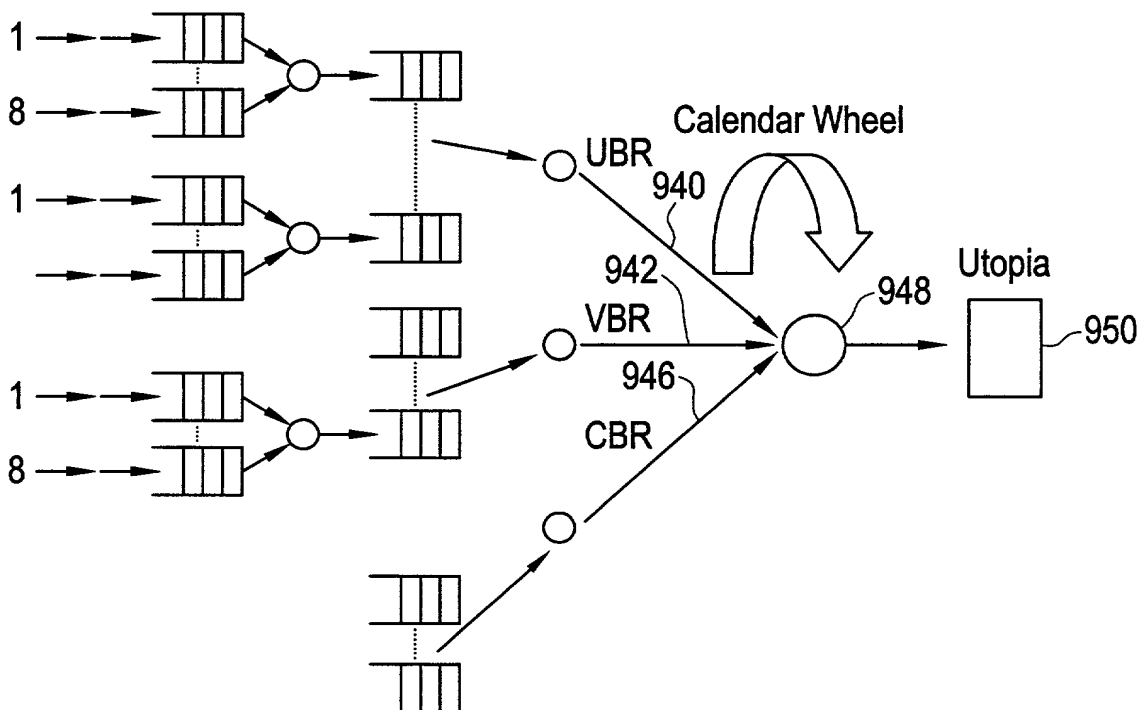


FIG. 76

960

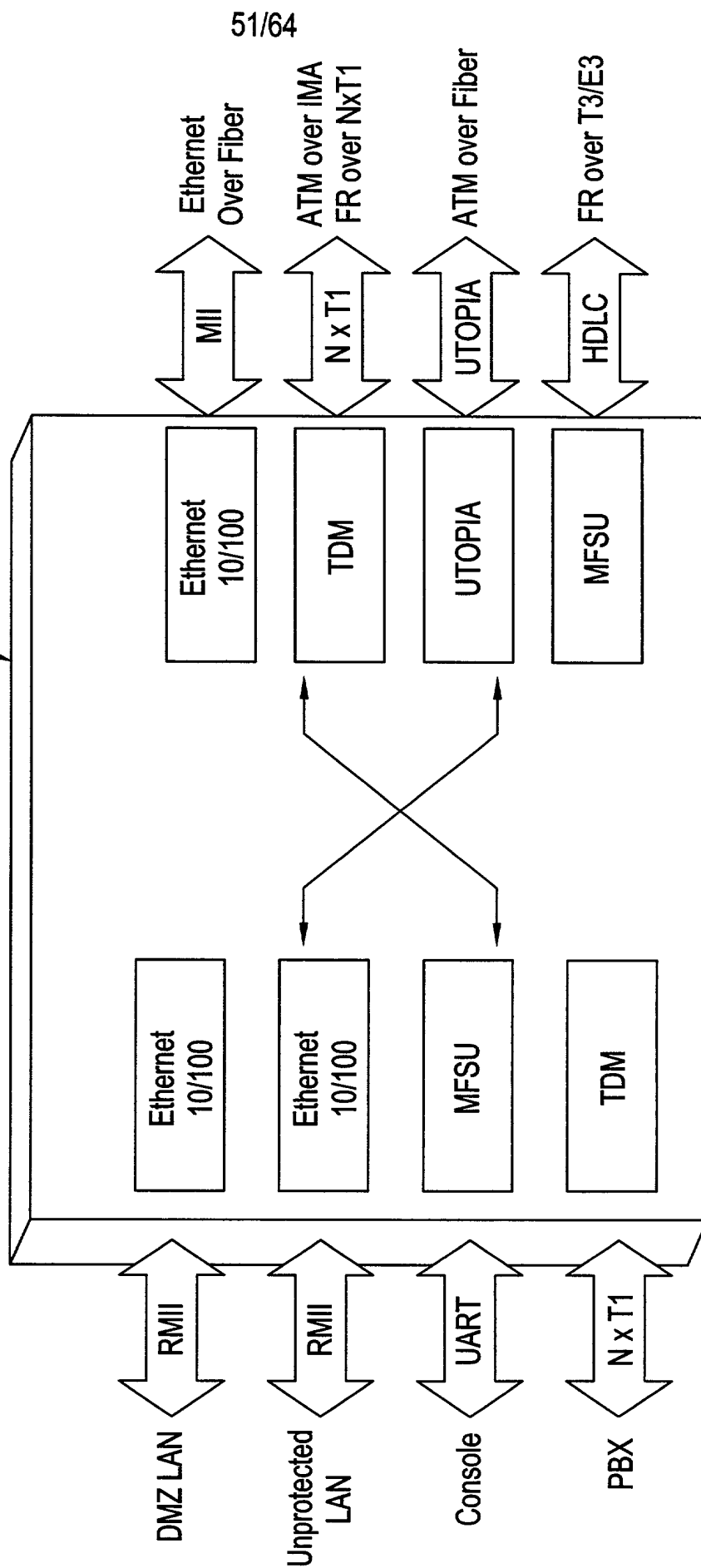


FIG. 77

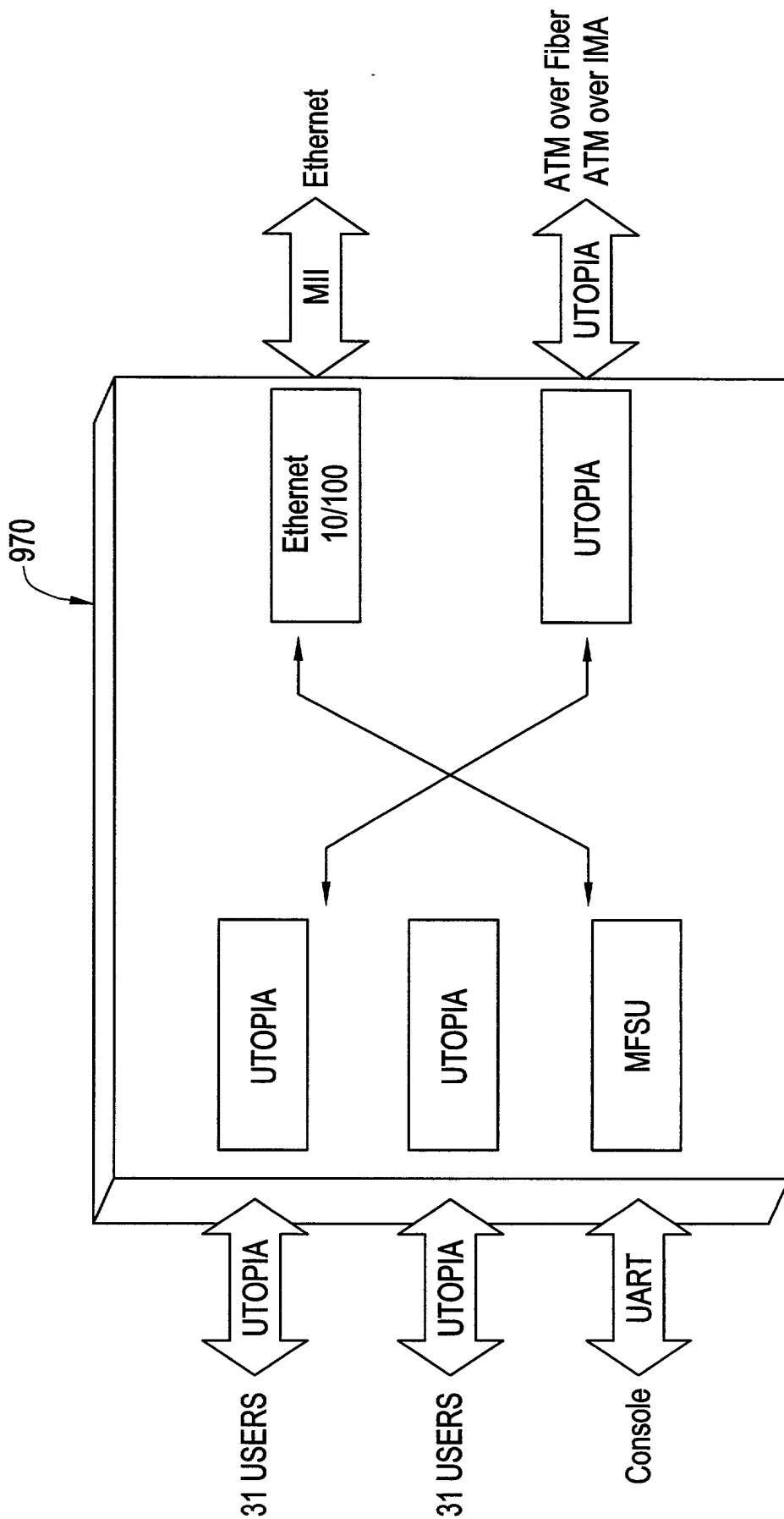


FIG. 78

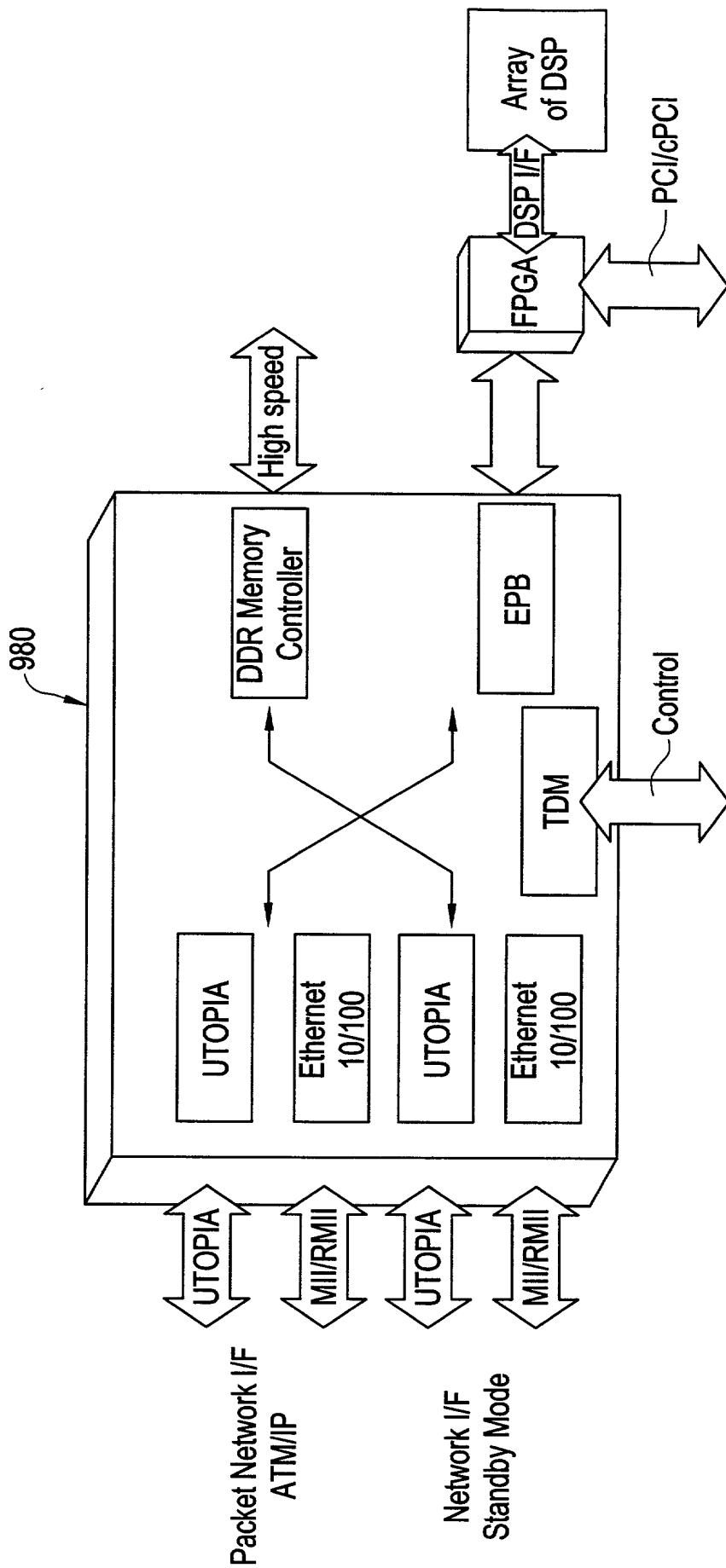


FIG. 79

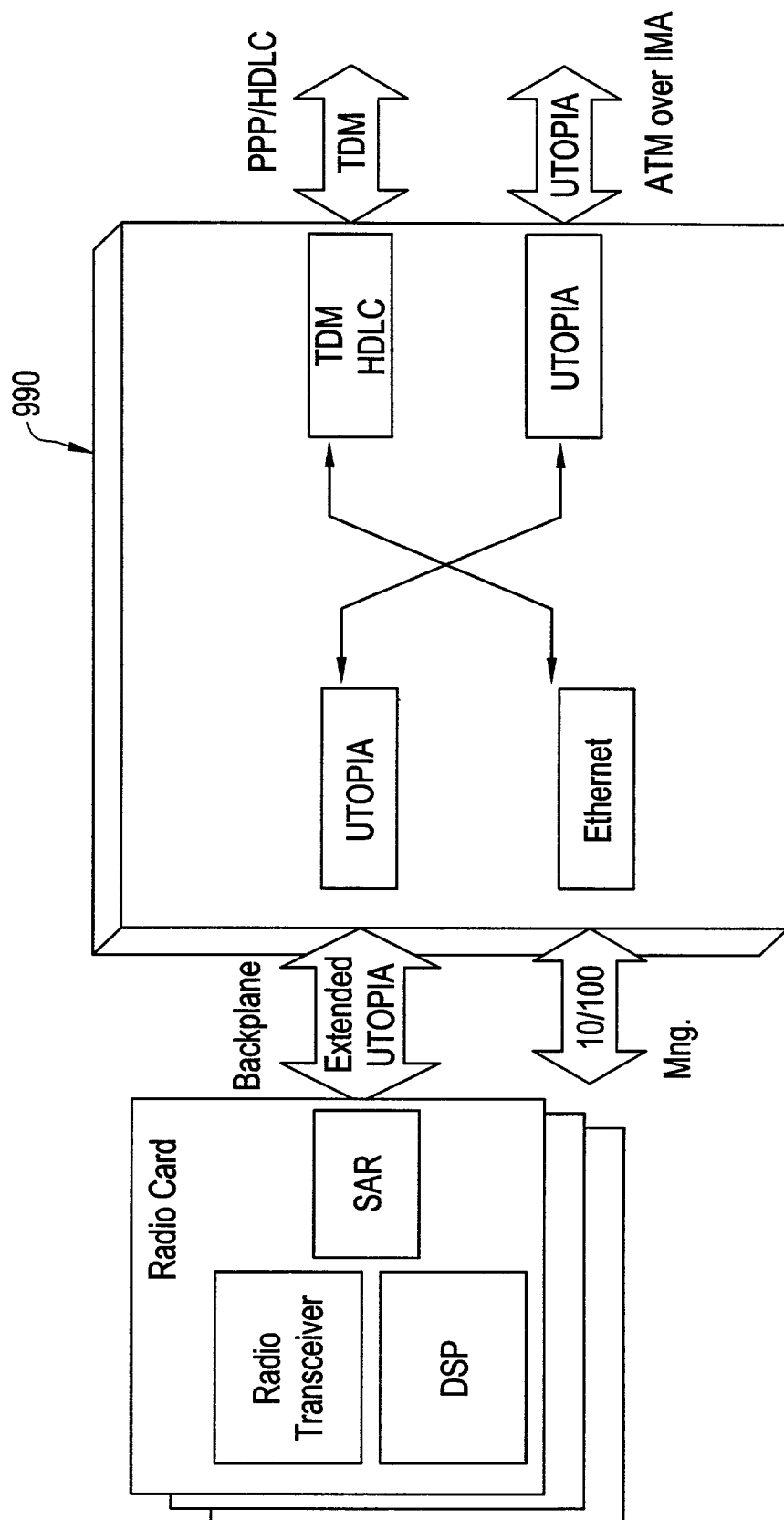


FIG. 80

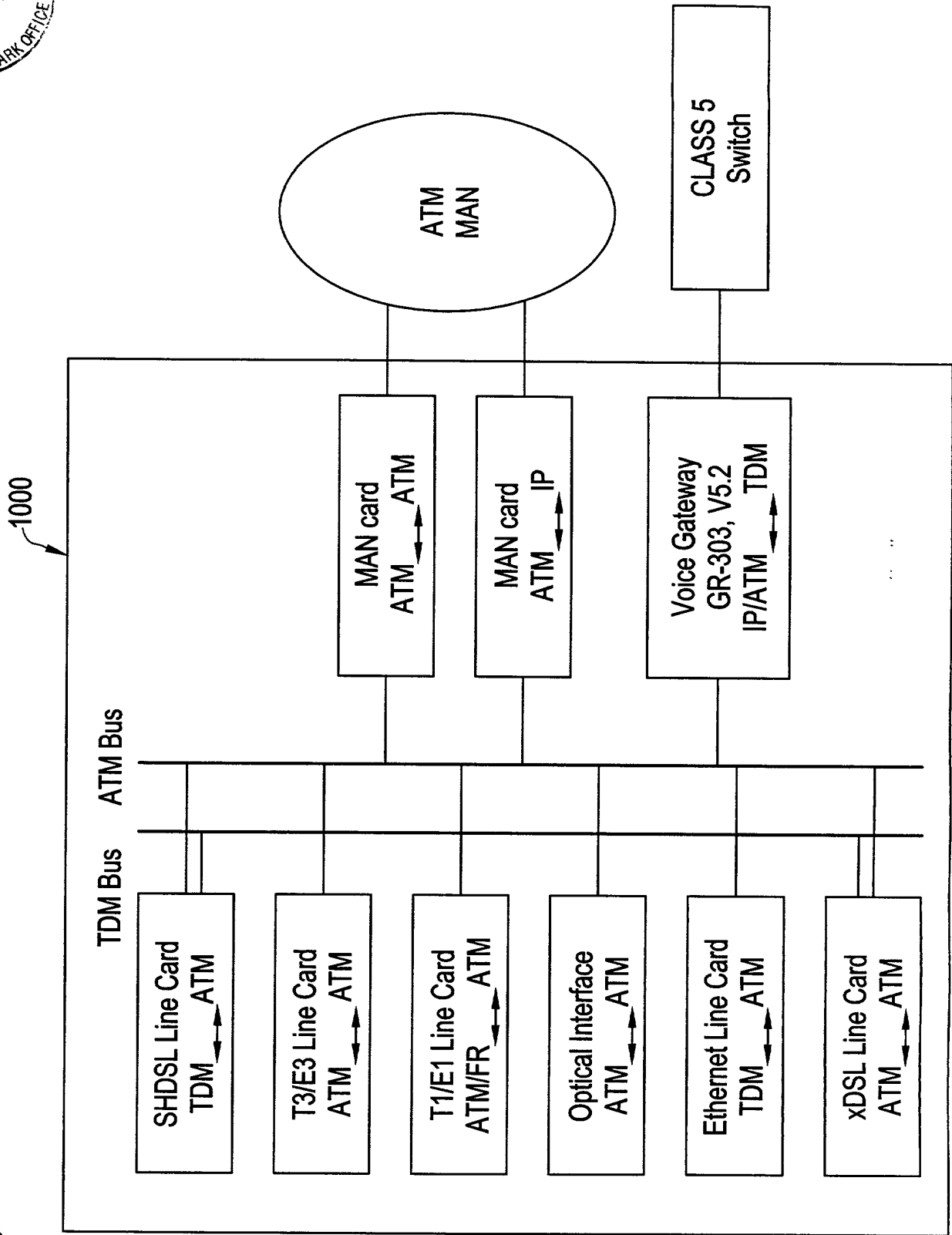


FIG. 81

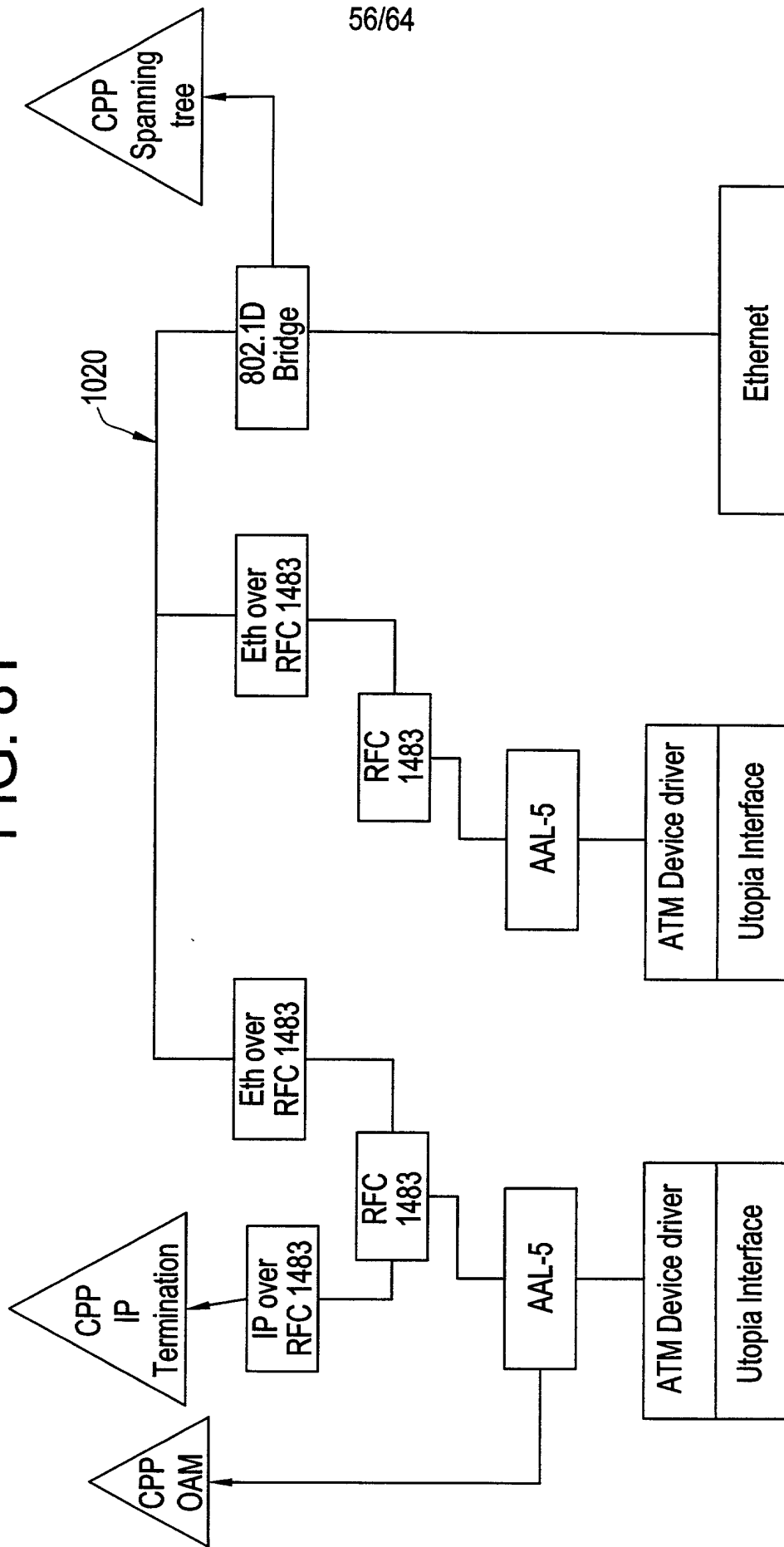


FIG. 82

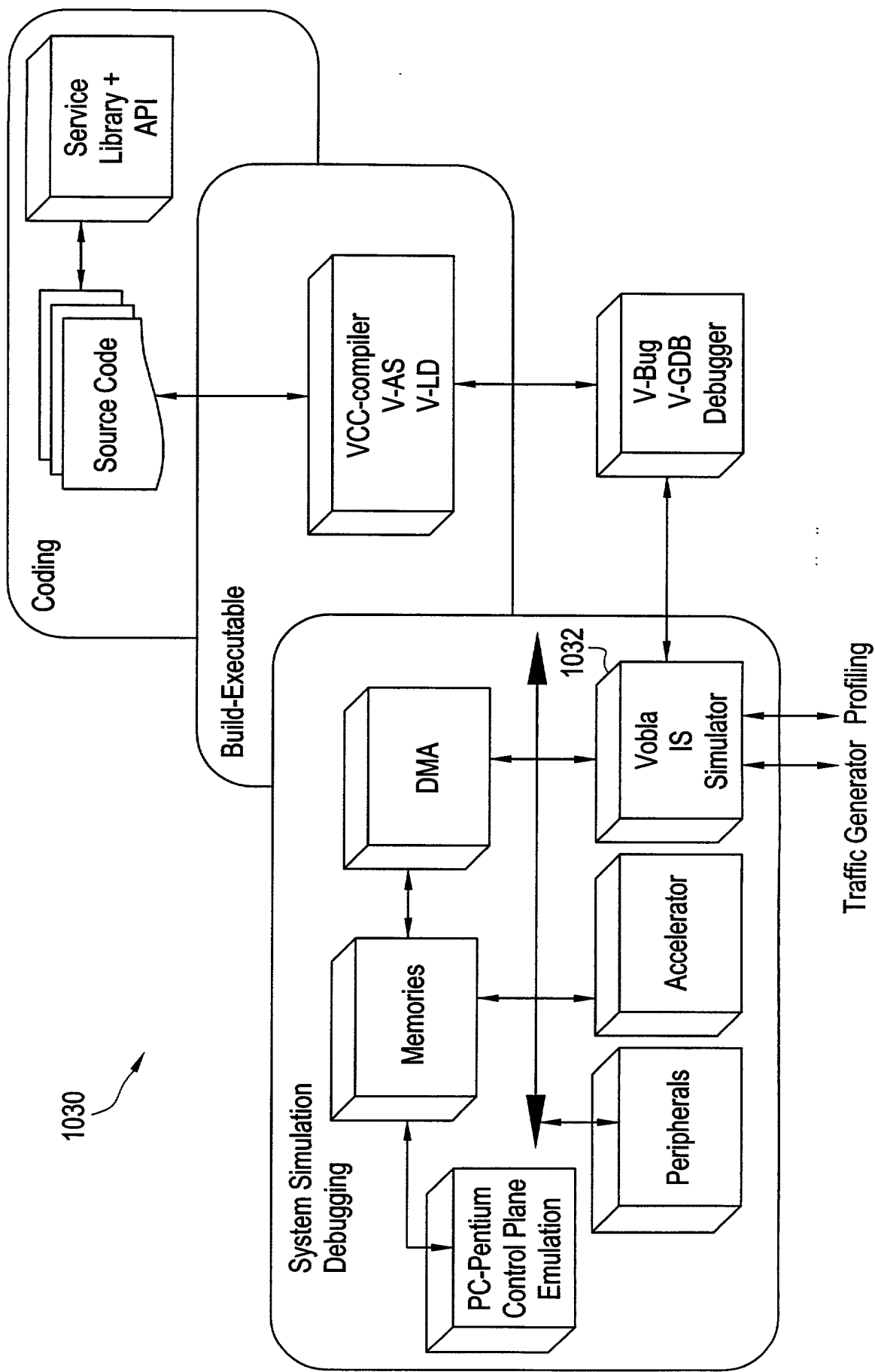


FIG. 83

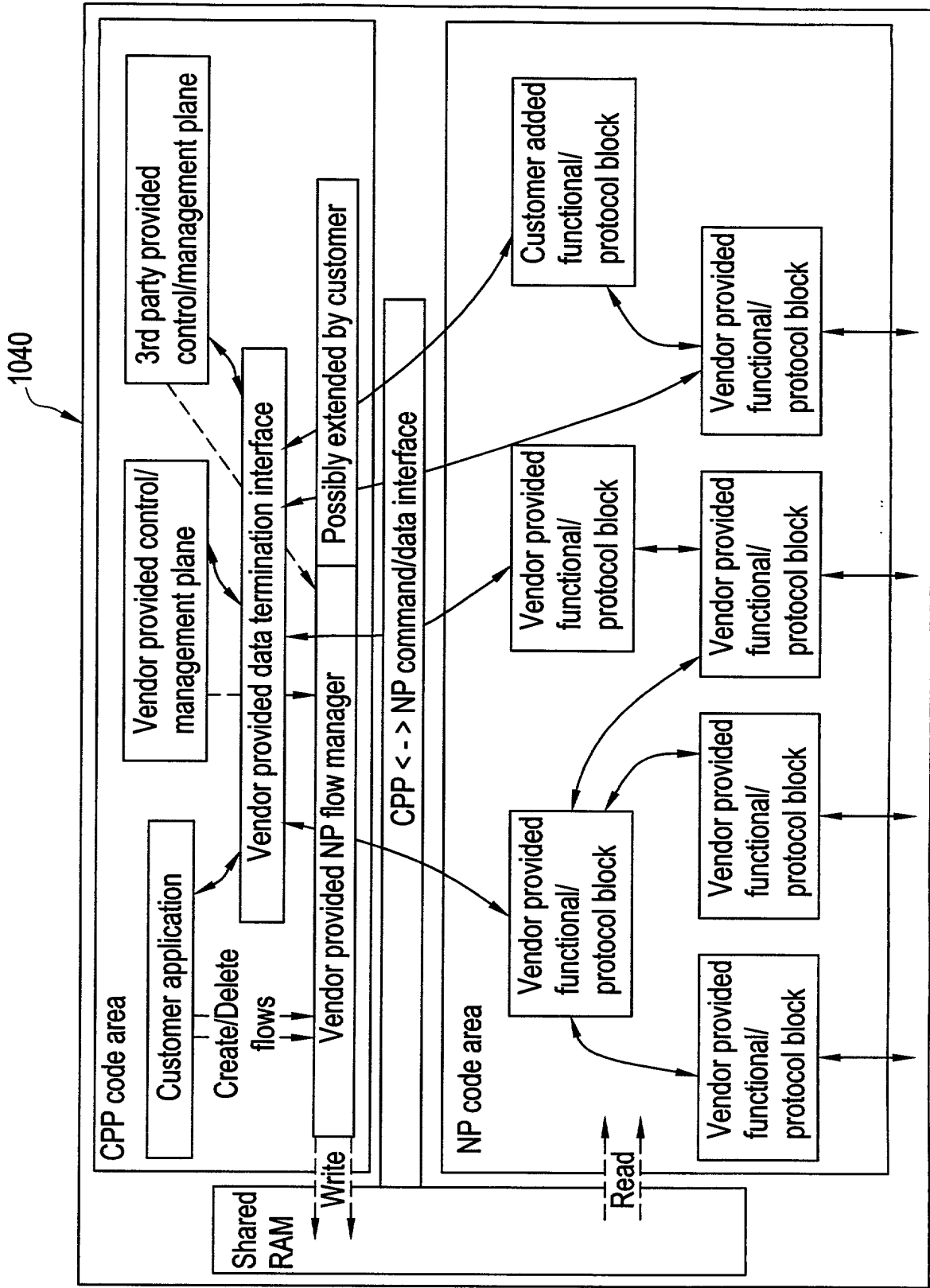


FIG. 84

1050

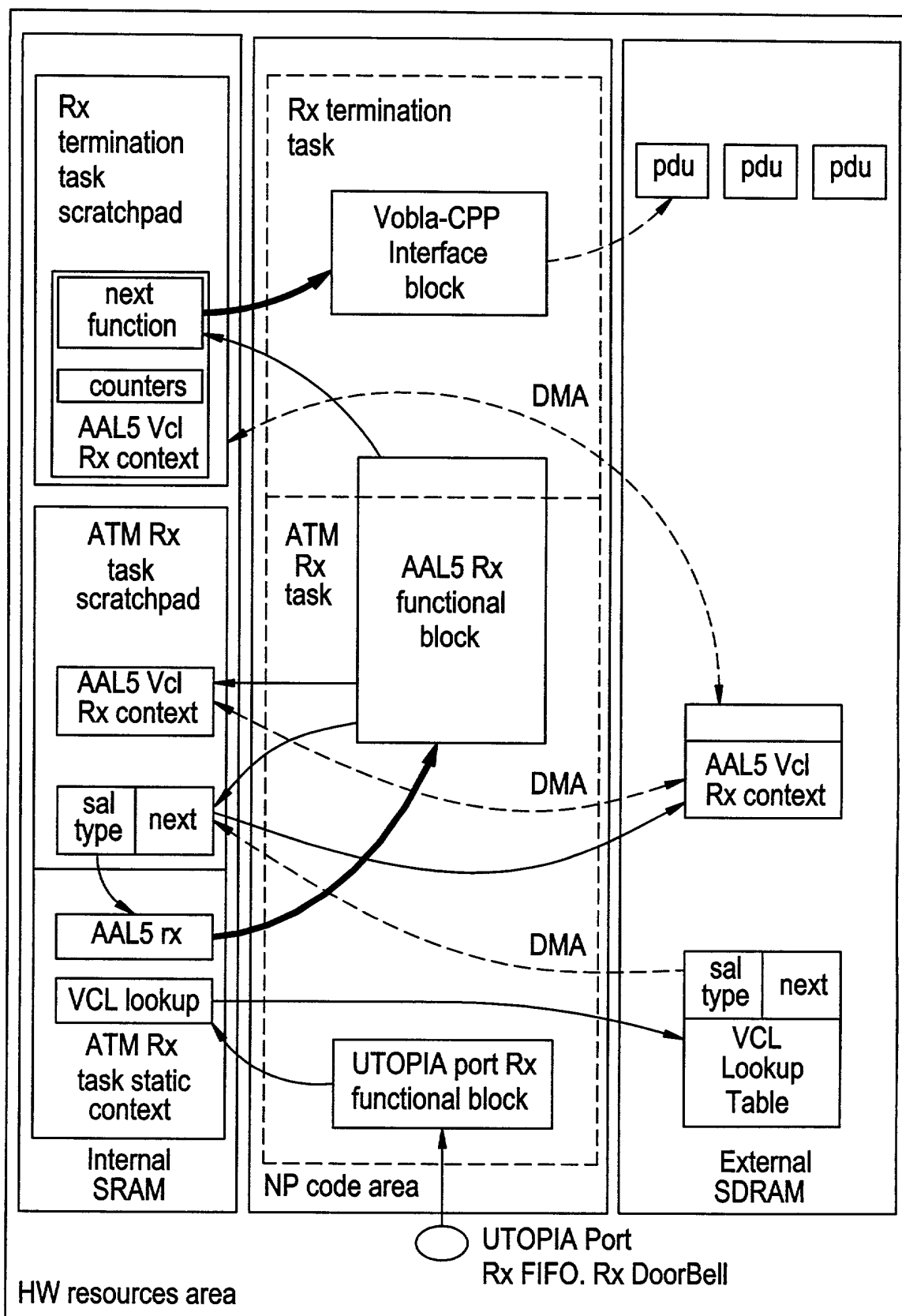


FIG. 85

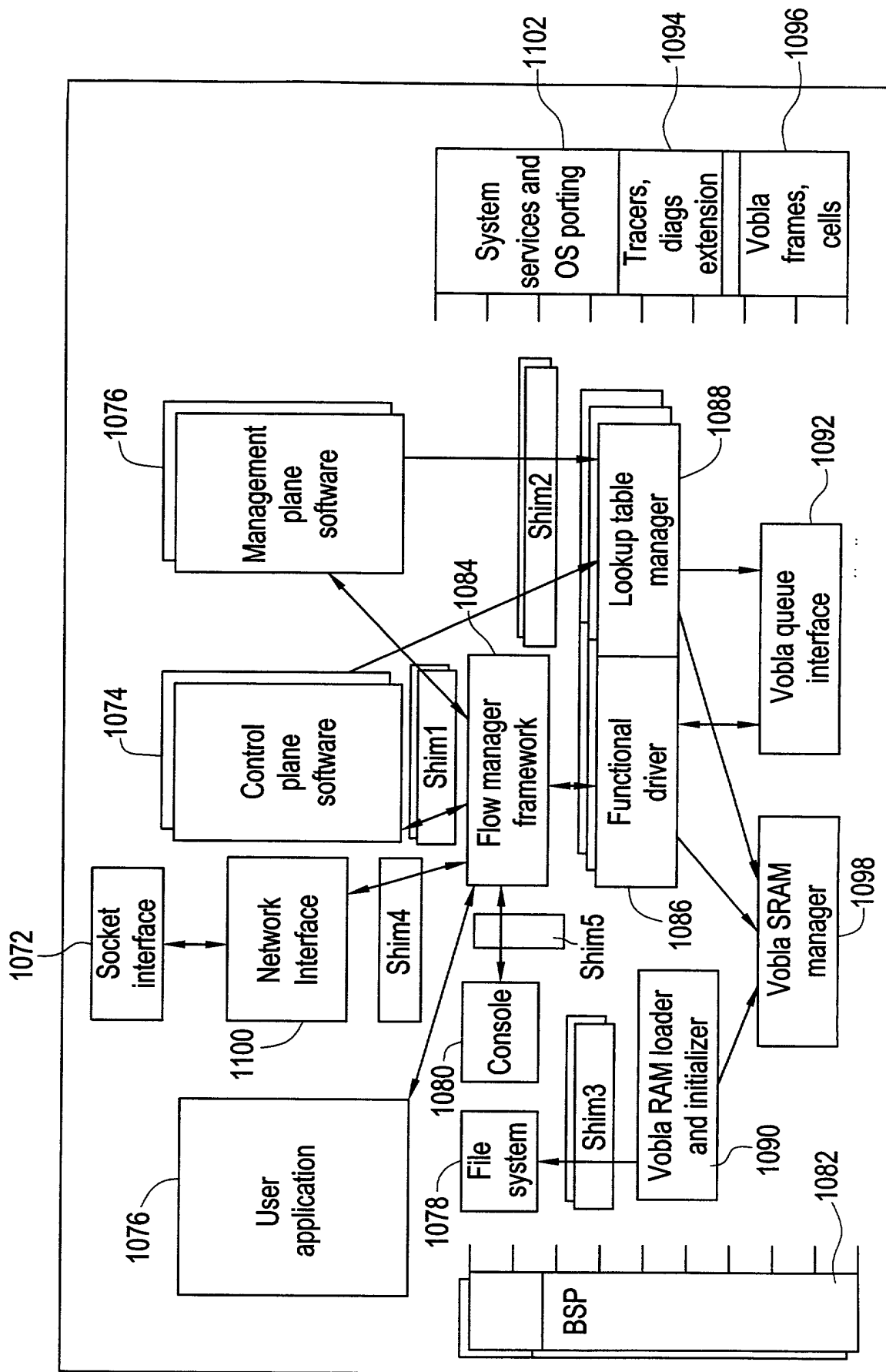


FIG. 86

1200

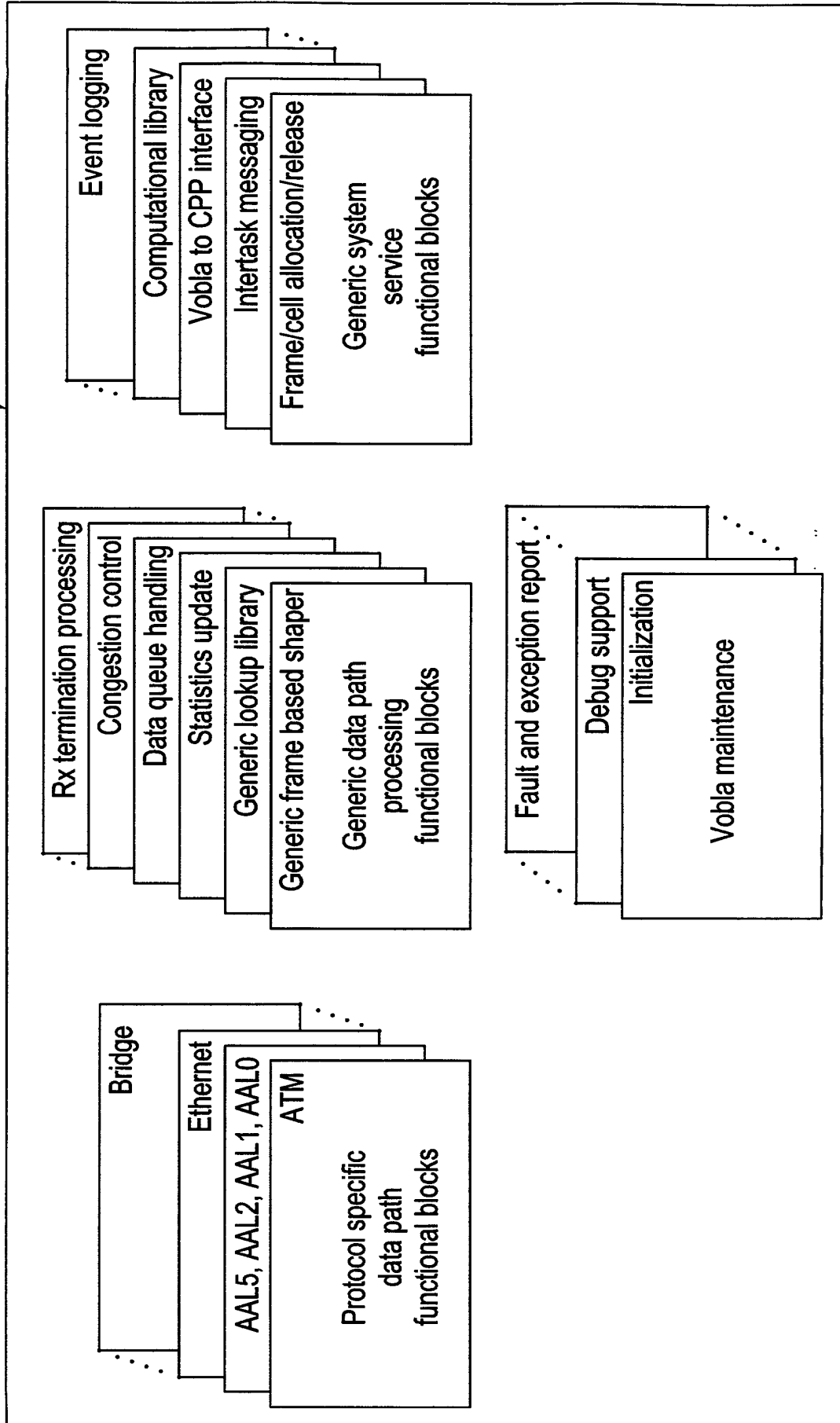


FIG. 87

PRIOR ART

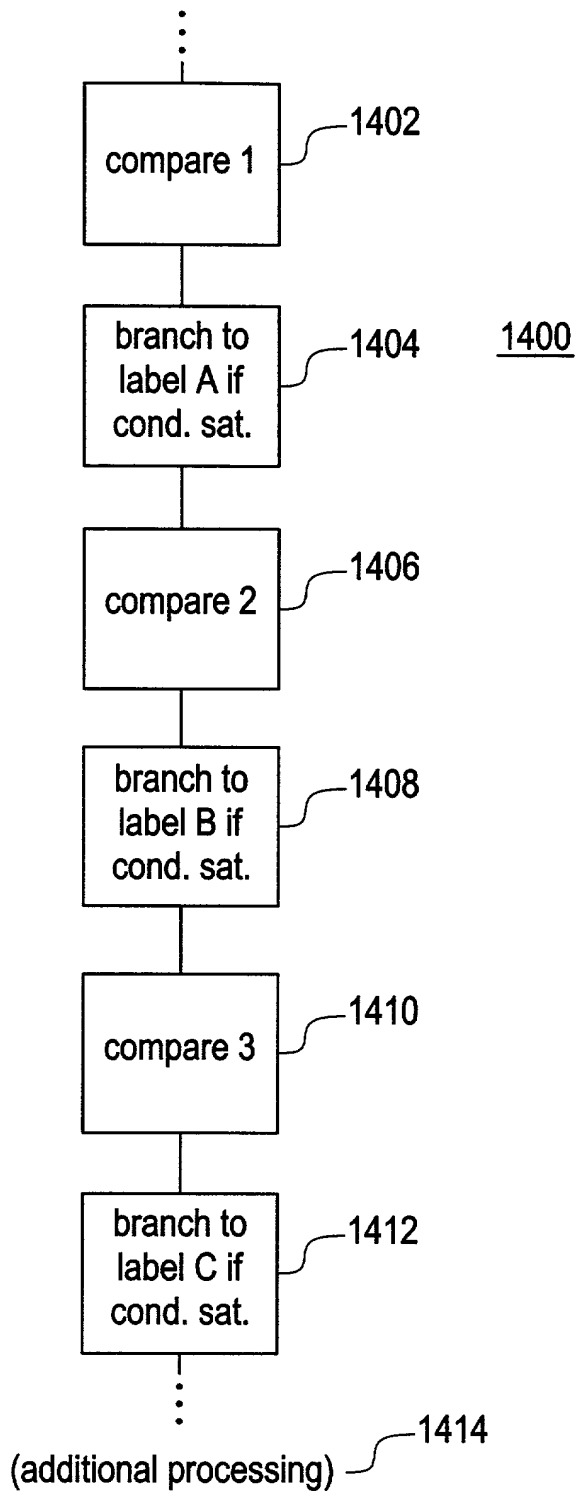


FIG. 88

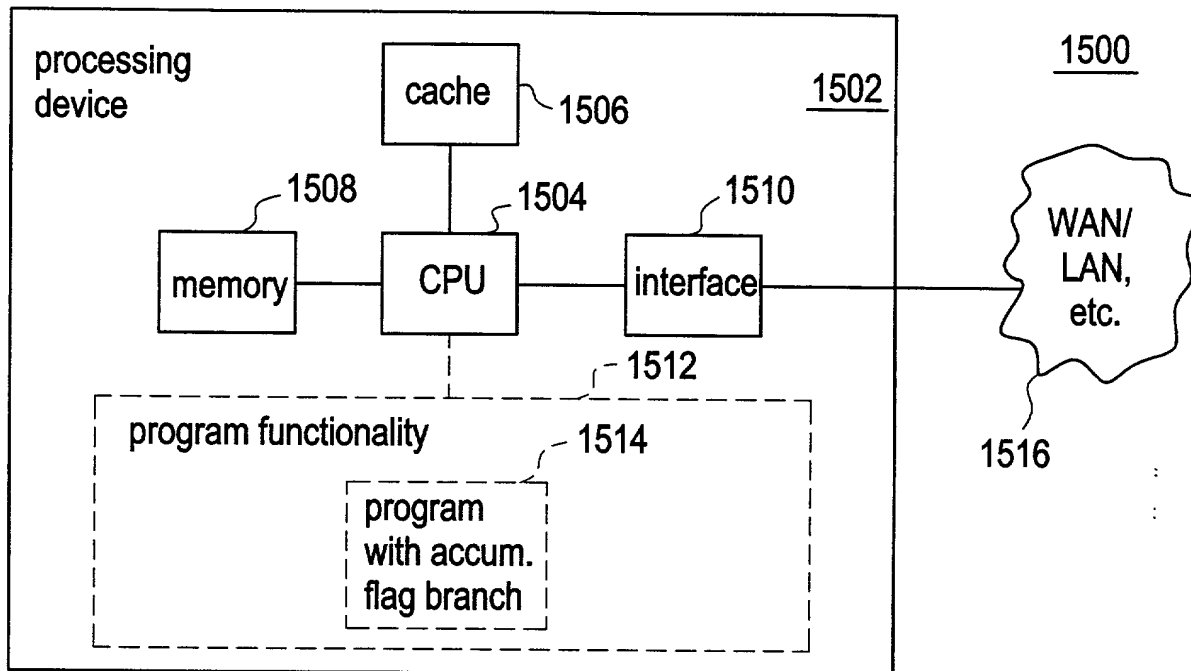
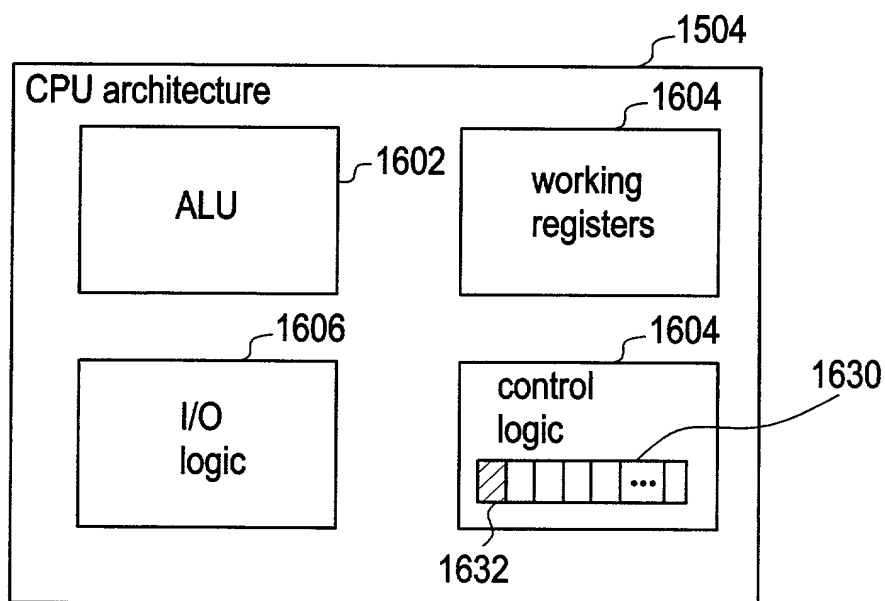


FIG. 89



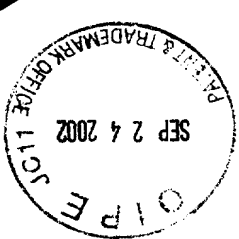


FIG. 90

